SEL-63-044

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SOLID-STATE ELECTRONICS LABORATORY

STANFORD ELECTRONICS LABORATORIES

STANFORD UNIVERSITY · STANFORD, CALIFORNIA

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Solid-State Electronics Laboratory
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Stanford University Stanford, California

## ABSTRACT

The field-effect transistor is treated from an active R-C transmission-line approach, and a circuit model is derived from a lumped-element approximation to the line. The circuit model is found to be similar to that often stated for the high-frequency (hf) circuit model of the vacuum tube. The model is characterized by the low-frequency (1-f) admittance parameters and two high-frequency parameters: the cutoff frequency (which is the frequency at which the hf transconductance falls to one-half of its 1-f value) and a constant relating to the input conductance. A maximum useful frequency for the device, which is close to the cutoff frequency, is calculated from the model. Measurements are found to be in agreement with the predictions of the theory for frequencies less than the cutoff frequency.

A noise model for the field-effect transistor is derived by assigning thermal-noise generators to the conductive elements of the transmission-line model and shot-noise generators to the gate junction. The input-noise current is then found to be proportional to the input conductance and leakage current, and the output-noise current is proportional to the output conductance, transconductance, and leakage current. This model is shown by experiment to be valid for frequencies where 1/f noise is not important.

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## ILLUSTRATIONS (Cont'd)

## ILLUSTRATIONS (Cont'd)

ACKNOWLEDGMENT

The author would like to acknowledge the stimulating guidance of Prof. Malcolm McWhorter in this study. The author is also indebted to the National Science Foundation which supported a portion of this research through its Graduate Fellowship Program.

# I. INTRODUCTION

The field-effect transistor, first proposed by W. Shockley, is a member of a class of semiconductor devices that may be called unipolar in contrast to the junction transistor whose working current is essentially bipolar. A distinguishing feature of the device is its close resemblance to a vacuum tube in terminal characteristics.

A dc analysis of the field-effect transistor has been carried out by Shockley [Ref. 1] and Dacey and Ross [Ref. 2], and small-signal circuit models were derived from this analysis. Experiments [Ref. 2] have verified the dc model, and the essential features of the small-signal models. However, no theory has been presented that explains the frequency behavior of all the two-port network parameters and, in particular, no detailed theory of device noise is available.*

In this report the field-effect transistor is analyzed from an active R-C transmission line viewpoint, and a circuit and noise model of the device is derived. This approach yields a circuit model that more accurately describes the device than does the previous model of Shockley [Ref. 1]. In addition a noise model is obtained that is valid throughout the useful frequency range of the device, and is not limited to low frequencies as is that of van der Ziel [Refs. 3,4]. Experimental confirmation of the models is also presented.

## A. A QUALITATIVE THEORY

The field-effect transistor (FET) consists of a layer of n-type semiconductor, with gate electrodes of p-type material either side of this layer.** One example of a field-effect transistor is shown in Fig. 1. A reverse bias is applied to the gate junctions and the resulting depletion (space-charge) regions cause the drain-to-source current to

*In Refs. 3 and 4, van der Ziel has discussed the noise-generating mechanisms in field-effect transistors for the case of low frequencies.

**The device may also be constructed with a p-type channel and an n-type gate.

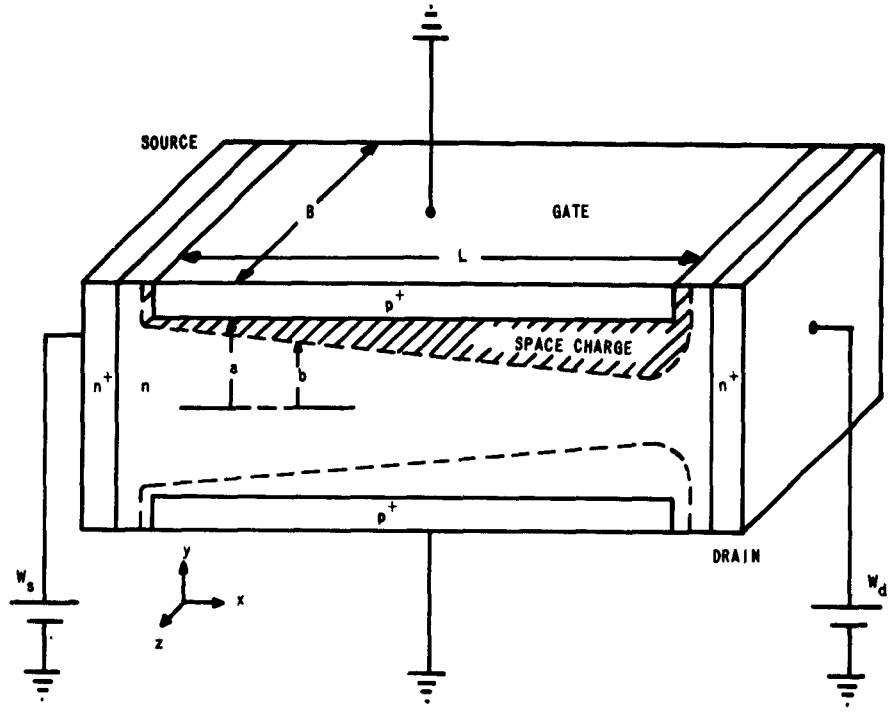


FIG. 1. A FIELD-EFFECT TRANSISTOR STRUCTURE.

flow in a channel bounded by these space-charge regions. If the voltage $W_d$ is greater than $W_s$, then the space-charge layer is wider at the drain than at the source.

Small-signal effects can be observed by inserting a signal between the gate and ground; the effect is to vary the width of the depleted region and hence to change the drain-to-source current. This is similar to a vacuum-tube triode where the grid voltage varies the plate current. Since the gate junction is reverse-biased it is in a high-impedance condition and the resemblance to the triode is even more complete. Typical values of transconductance range from 100 to 5000 μmhos, with input impedances of several megohms or greater.

Other structures are possible that use a "gate" charge to control a "channel" current but do not use p-n junctions. One of the earlier

attempts used the surface of a semiconductor: a thin insulating layer was used between the semiconductor and a conducting layer. A potential is applied across the insulator and the change in gate charge would change the number of electrons and holes at the surface, thus altering the conductivity of the layer. This device has been the object of recent investigations.* Since this device is also unipolar in that the channel current is a majority-carrier current, and this current is modulated by the action of the gate capacitance, the analyses to be presented in Chapters III and IV should also apply. However, for simplicity, the physical model to be used is the field-effect transistor of Shockley.

## B. SUMMARY OF CONTENTS

The mathematical analysis of the dc operation of the FET is discussed in Chapter II. In addition a small-signal circuit model is derived from the dc characteristics. Corrections to this "ideal" theory, such as high-field effects and gate junction impedances are discussed and are shown to result in an amended circuit model. Experimental results of previous investigators are briefly mentioned.

In Chapter III the device is analyzed on the basis of a lumped R-C transmission line. A pi-section circuit model, valid throughout the useful frequency range of the device, is derived from the transmission line model and is shown to resemble closely the high-frequency circuit model of the vacuum tube. A maximum useful frequency for the device is defined and calculated from the model. Measurements are found to agree with the theory.

In Chapter IV a noise model is derived from the circuit model of Chapter III. This model is used to determine the noise factor of the device and an optimum environment. Measurements confirm the essential features of the theory.

Chapter V contains some conclusions concerning application of the various models and some suggestions for further study.

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*M. M. Atalla, Solid State Device Research Conference, Pittsburgh, June 1960; P. K. Weimer, Solid State Device Research Conference, Stanford University, June 1961.

## II. THE PHYSICAL THEORY OF OPERATION

The low-frequency theory of the field-effect transistor of Shockley is presented for completeness. Modifications to the ideal theory are discussed and the results of previous investigators are related to the theory.

### A. PHYSICAL THEORY OF THE UNIPOLAR FIELD-EFFECT TRANSISTOR [Ref. 1]

A unipolar field-effect transistor, together with a biasing arrangement, is shown in Fig. 1.

If the electric field in the channel is small, the current through the channel is

$$I = 2Bb\sigma_o E_x = g(W)E_x \tag{2.1}$$

where $\sigma_o$ is the conductivity of the channel, B is the width of the device, and W is the magnitude of reverse bias along the channel, measured with respect to the gate. The assumption that the electric field $E_x$ is small is called the gradual approximation; it allows one to calculate b, the half-width of the channel, on the basis of a depletion layer at the gate which is reverse biased with a voltage W.* Then a simple calculation shows**

$$b = a\left[1 - \left(\frac{W}{W_o}\right)^{\frac{1}{2}}\right] \tag{2.2}$$

where a is the zero-bias half-width of the channel and $W_o$ is the potential required to pinch off the channel, that is, to cause the two

---

*The gradual approximation in essence says that the potential at x is determined by the charge at x and not by charges lying to either side. The electric field $E_x$ should be less than the field across the junction, or $10^4$ v/cm.

**The exponent of $W/W_o$ depends on the gradation of impurities at the gate junction. For a step junction the exponent is 1/2; for a linearly graded junction the exponent is 1/3. In the succeeding analysis a step junction is assumed.

space-charge regions at the gate to meet at the center of the channel. Substituting (2.2) into (2.1) and recognizing that $E_x = dW/dx$, we obtain the following integral equation for $I_d$, the drain current:*

$$I_d = \frac{1}{L} \int_{W_s}^{W_d} g(W)\, dW \tag{2.3}$$

where

$$g(W) = 2\sigma_o\, aB\left[1 - \left(\frac{W}{W_o}\right)^{1/2}\right] = g_o\left[1 - \left(\frac{W}{W_o}\right)^{1/2}\right] \tag{2.4}$$

Integrating, we obtain

$$I_d = \frac{g_o}{L}\left\{W_d - W_s + \frac{2}{3}W_o\left[\left(\frac{W_s}{W_o}\right)^{3/2} - \left(\frac{W_d}{W_o}\right)^{3/2}\right]\right\} \tag{2.5}$$

In terms of the terminal voltages $V_g$, $V_s$, $V_d$

$$W_s = V_s - V_g \tag{2.6a}$$

$$W_d = V_d - V_g \tag{2.6b}$$

$$I_d = \frac{g_o}{L}\left\{V_d - V_s + \frac{2}{3}W_o\left[\left(\frac{V_s - V_g}{W_o}\right)^{3/2} - \left(\frac{V_d - V_g}{W_o}\right)^{3/2}\right]\right\} \tag{2.7}$$

The current reaches a maximum at $V_s + V_d = W_o$ and remains essentially constant at a value $I_{do}$ after that. It should be noted here that the gradual approximation fails near pinch-off. The result is to cause a small positive slope to the $I_d - V_d$ characteristic, resulting in a high (but not infinite) drain resistance. The output characteristic of (2.7) is shown in Fig. 2 with $V_s = 0$ and $V_g$ a parameter.

*This equation assumes current continuity; we are thus neglecting gate currents. If the gate current is small compared to the drain current, then we can add it later and not disturb the potential in the channel.

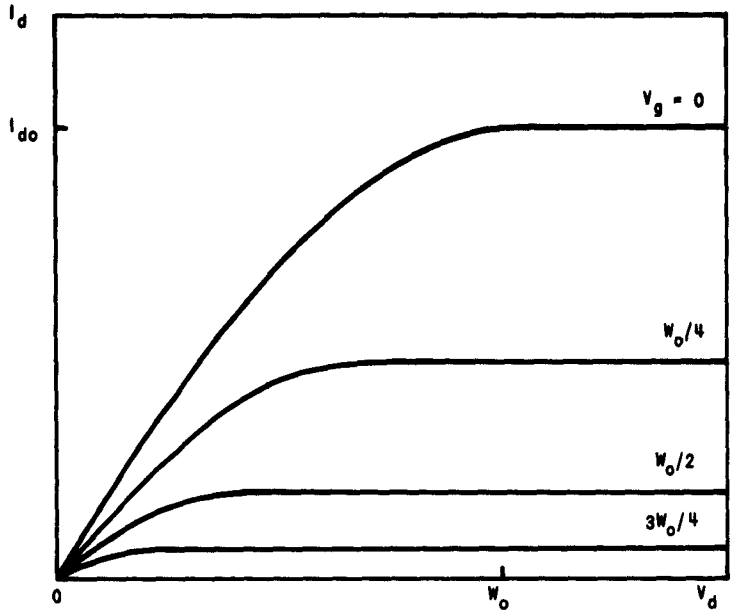



FIG. 2. OUTPUT CHARACTERISTICS OF THE FIELD-EFFECT TRANSISTOR.

The small-signal behavior is obtained from (2.4) by making small changes $v_g$, $v_d$, $v_s$ in the terminal voltages. The change $i_d$ in $I_d$ is then

$$i_d = \frac{g_d}{L}\delta W_d - \frac{g_s}{L}\delta W_s = \frac{g_d}{L}v_d - \frac{g_s}{L}v_s - \left(\frac{g_d - g_s}{L}\right)v_g \qquad (2.8)$$

where

$$g_s = g\,(W_s) = g\,(V_s - V_g) \qquad (2.9a)$$

$$g_d = g\,(W_d) = g\,(V_d - V_g) \qquad (2.9b)$$

Equation (2.8) can be put into a form recognizable as the current equation for a vacuum-tube triode:

$$i_p = g_m\left(v_g - v_c + \frac{v_p - v_c}{\mu}\right) \qquad (2.10)$$

Comparing (2.9) and (2.10) we find

$$g_m = \frac{g_d - g_s}{L} \triangleq G_m \tag{2.11a}$$

$$r_p = \frac{L}{g_d} \triangleq \frac{1}{G_d} \tag{2.11b}$$

$$\mu = - g_m r_p = \frac{g_d - g_s}{g_d} \tag{2.11c}$$

We can rewrite (2.8) as

$$i_d = G_m \left( v_g - v_s + \frac{v_d - v_s}{\mu} \right) \tag{2.12}$$

From this equation the close resemblance of the terminal characteristics of the FET and the vacuum tube is seen.

There will also be a capacitance associated with the gate. According to Shockley the frequency response is limited by the time needed to charge this gate capacitance, $C_g$, through a resistance $R$ of the channel between the gate and source. From these considerations one can infer the circuit model shown in Fig. 3.

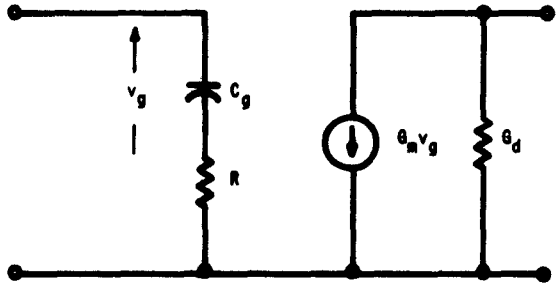



FIG. 3. CIRCUIT MODEL BASED ON SHOCKLEY'S THEORY.

As Eqs. (2.9) imply, the small-signal parameters depend upon the terminal biases. From (2.4) and (2.11) we find

$$G_m = \frac{g_o}{L}\left[\left(\frac{V_d - V_g}{W_o}\right)^{1/2} - \left(\frac{V_s - V_g}{W_o}\right)^{1/2}\right] \tag{2.13a}$$

$$G_d = \frac{g_o}{L}\left[1 - \left(\frac{V_d - V_g}{W_o}\right)^{1/2}\right] \tag{2.13b}$$

$$\mu = -\frac{\left(\frac{V_d - V_g}{W_o}\right)^{1/2} - \left(\frac{V_s - V_g}{W_o}\right)^{1/2}}{1 - \left(\frac{V_d - V_g}{W_o}\right)^{1/2}} \tag{2.13c}$$

Equation (2.11) and (2.12) are valid up to the pinch-off point and remain constant thereafter. Equation (2.13) predicts an infinite voltage amplification at pinch-off. This, of course, is not true and is a result of failure of the gradual approximation at the drain end of the channel. Measurements show that $\mu$ does remain finite at pinch-off. The capacitance depends on the width of the depletion region at the gate, which in turn is proportional to the square root of the voltage across the gate junction.

## B. EFFECT OF LARGE CHANNEL FIELDS [Ref. 2]

For electric fields of the order $10^3$ v/cm and higher, the mobility of carriers in germanium and silicon decreases. The effect of this decrease in mobility can be accounted for by introducing a field-dependent channel conductivity. The result of this nonlinearity is to change the bias dependence of the small-signal parameters calculated previously; however, the circuit model of Fig. 3 is not changed.

Comparing (2.9) and (2.10) we find

$$g_m = \frac{g_d - g_s}{L} \triangleq G_m \tag{2.11a}$$

$$r_p = \frac{L}{g_d} \triangleq \frac{1}{G_d} \tag{2.11b}$$

$$\mu = - g_m r_p = \frac{g_d - g_s}{g_d} \tag{2.11c}$$

We can rewrite (2.8) as

$$i_d = G_m \left( v_g - v_s + \frac{v_d - v_s}{\mu} \right) \tag{2.12}$$

From this equation the close resemblance of the terminal characteristics of the FET and the vacuum tube is seen.

There will also be a capacitance associated with the gate. According to Shockley the frequency response is limited by the time needed to charge this gate capacitance, $C_g$, through a resistance R of the channel between the gate and source. From these considerations one can infer the circuit model shown in Fig. 3.

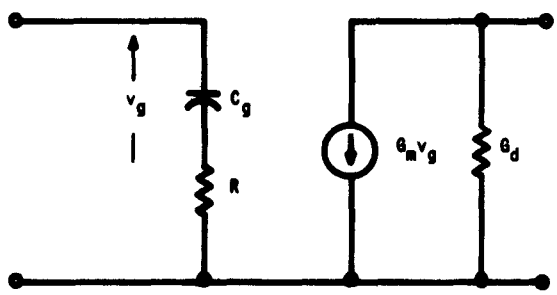



FIG. 3. CIRCUIT MODEL BASED ON SHOCKLEY'S THEORY.

## C. EFFECT OF INTRINSIC LEAD RESISTANCES

The effect of series resistance in the source and drain leads on the performance of the device can be included by adding these elements to the circuit model of Fig. 3. The most serious effect is caused by resistance in the source lead. This reduces the transconductance in a similar manner to cathode degeneration in a vacuum-tube triode. The series resistances also cause dc voltage drops that reduce the bias on the ideal device.

## D. THE GATE JUNCTION

In calculating the drain characteristic of Fig. 2 we have neglected the dc current that flows through the gate junction. As the junction is reverse biased, this current is small (on the order of 1 μamp for germanium devices, 10 nanoamp, or less, for silicon units). In any event the effect of this current is to cause the current in the channel to vary with $x$, and as a result, Eq. (2.4) is not exactly correct. The error, however, is negligible due to the smallness of the gate current under usual bias conditions.

In addition to capacitance, the gate junction contains a leakage resistance $R_g$; this resistance can be calculated from

$$R_g = \frac{\partial V_g}{\partial I_g} \tag{2.14}$$

The leakage resistance is determined by the mechanism causing $I_g$. The gate current has two components: a diffusion component and a space-charge generation current. In a reverse-biased germanium p-n junction the diffusion component predominates and is independent of applied voltage: therefore an extremely high resistance (ideally infinite) results. For a silicon p-n junction, space-charge generation of carriers predominates, giving rise to a current which is proportional to the volume of the space-charge region. For a step junction the volume is proportional to the square root of the gate voltage. It follows that

$$I_g = kV_g^{1/2} \tag{2.15}$$

Although this current does not saturate as does a diffusion current, the resistance of the junction is still quite high. The resistance is calculated from (2.14):

$$R_g = \frac{2V_g}{I_{go}} \tag{2.16}$$

where $I_{go}$ is the dc leakage current. As an example, let $V_g = 1$ v and $I_{go} = 1$ nanoamp. Then $R_g$ is about $10^9$ ohms.

## E. PREVIOUS EXPERIMENTAL RESULTS

At the time Shockley published his original theory, no experimental evidence was presented. Later Dacey and Ross constructed several devices and found agreement of dc characteristics with Shockley's theory. Their devices were constructed of germanium and were found to obey the nonlinear mobility case. No detailed frequency measurements were reported; only a maximum frequency of oscillation was measured, using a unity-coupled oscillator. This frequency was found to agree (within 150 percent in some cases) with a frequency found by considering the time constant of the gate.

Later measurements of field-effect transistors were reported by Huang, Marshall, and White [Ref. 5], who considered applications of the devices. The admittance parameters were measured, but no model was devised to explain their behavior.

Noise measurements were made by Dacey and Ross, who reported 70-db noise figures for germanium devices. The newer silicon units have been reported to have noise figures as low as 0.4 db at 1 kc with source resistances of 1 megohm [Ref. 6]. Lauritzen suggested a high-field phenomenon as the source of noise in the channel, and leakage currents as a source of gate noise. However no detailed calculations were stated.

## III. A CIRCUIT MODEL

This chapter introduces a transmission-line approach to the FET. A lumped-element approximation is made to the distributed line and a pi-section circuit model is derived from this approximation. A maximum useful frequency is defined and calculated. Experimental results are shown to agree closely with the theory over the useful frequency range of the device.

### A. THE TRANSMISSION-LINE APPROACH

Many semiconductor devices have been treated from a transmission-line approach. The base region of a junction transistor is a well-known example. A device similar in structure to the FET has been analyzed and shown to have a notch filter characteristic.*

On an intuitive basis one can draw the transmission-line model of the FET as shown in Fig. 4. This model represents the small-signal behavior of the device. The series resistance of the channel acts as series R and the gate capacitance acts as shunt C. In addition, the device is active; therefore, we must augment our model with an active element.

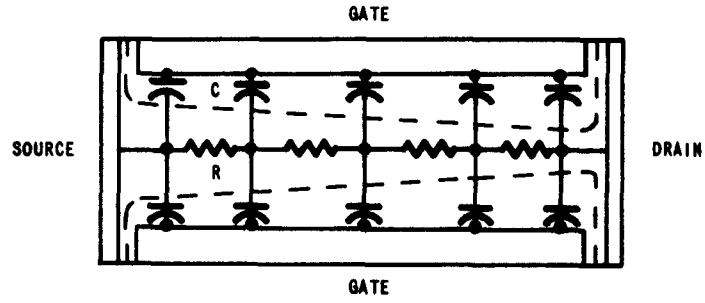



FIG. 4. AN FET STRUCTURE SHOWING LUMPED R AND C ELEMENTS OF TRANSMISSION-LINE MODEL.

*The device is essentially a field-effect transistor, operated with zero drain voltage (and therefore no gain) in a common gate mode. See Ref. 7.

This is easily done by noting that R is dependent on the gate voltage. A small variation in the gate voltage produces a small change in the resistance, which in turn varies the current flowing in the channel. A current generator, i, can be added in parallel with R that reproduces this current variation. A section of the augmented line is shown in Fig. 5.

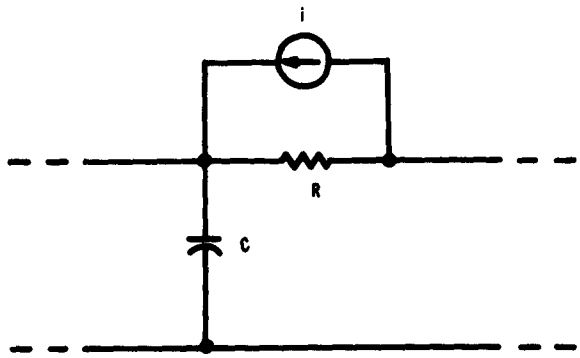



FIG. 5. A SECTION OF THE AUGMENTED TRANSMISSION-LINE MODEL OF FIG. 4.

## B. A WAVE EQUATION FOR THE FET

Consider Fig. 6. The current through the section I is equal to the average conductance of the section times the voltage across the section:

$$I(x) = 2\sigma_o B \frac{b(x) + b(x + \Delta x)}{2\Delta x} [W(x) - W(x + \Delta x)] \qquad (3.1)$$

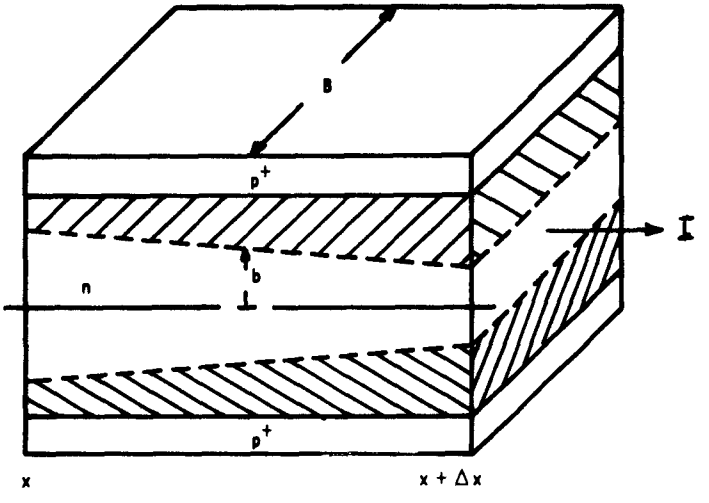



FIG. 6. A SECTION OF THE FET STRUCTURE OF FIG. 1.

Taking the limit as $\Delta x$ approaches zero, (3.2) results:

$$I(x) = -2\sigma_o B b(x) \frac{dW}{dx} \tag{3.2}$$

which is the same as (2.1). As we found in Chapter II, $b$ is also a function of $W$. To examine small-signal effects, expand $b$ in a Taylor series about the dc potential in the channel $V'$; let

$$W = V' + v$$

$$I = I' + i$$

where $v$ and $i$ are small ac voltages; $V'$ and $I'$ are the dc components of voltage and current in the channel. Then

$$b(x) = b[V'(x)] + \frac{db(V')}{dW} v(x) \tag{3.3}$$

where only the first two terms of the series are retained. Substituting (3.3) into (3.2)

$$- I(x) = 2\sigma_o Bb(V') \frac{d(V' + v)}{dx} + 2\sigma_o B \frac{db(V')}{dW} v(x) \frac{d(V' + v)}{dx}$$

Separating the dc terms and the ac terms we obtain

$$-I'(x) = 2\sigma_o Bb(V') \frac{dV'}{dx} \tag{3.4}$$

$$-i(x) = 2\sigma_o Bb(V') \frac{dv}{dx} + 2\sigma_o B \frac{db(V')}{dW} \frac{dV'}{dx} v(x) + 2\sigma_o B \frac{db(V')}{dW} v(x) \frac{dv}{dx} \tag{3.5}$$

Equation (3.4) is the same as (2.1), viz., the dc case. Equation (3.5) can be simplified somewhat by dropping the second-order term

$$2\sigma_o B \frac{db}{dW} v \frac{dv}{dx}$$

and recognizing that

$$\frac{db}{dW} \frac{dV'}{dx} \cong \frac{db}{dx}$$

Thus the ac current in the channel is

$$-i(x) = 2\sigma_o Bb \frac{dv}{dx} + 2\sigma_o B \frac{db}{dx} v = 2\sigma_o B \frac{d}{dx} bv$$

Defining $g = 2\sigma_o Bb$, as before,

$$-i(x) = \frac{d}{dx} gv \tag{3.6}$$

We have neglected the displacement current through the gate. Continuity requires that

$$\frac{di}{dx} = -c \frac{dW}{dt} = -c \frac{dv}{dt} \tag{3.7}$$

where $c$ is the capacitance of the gate electrode per unit length. Differentiating (3.6) and setting it equal to (3.7) we obtain the wave equation for the FET:

$$\frac{d^2}{dx^2} gv = \frac{c}{g} \frac{d}{dt} gv \tag{3.8}$$

We now assume a time dependence for $v$ as follows:

$$v = Ve^{j\omega t}$$

where $V$ is the magnitude of the ac voltage and $\omega$ is angular frequency. Then (3.8) becomes

$$\frac{d^2 gV}{dx^2} = j\omega \frac{c}{g} gV \tag{3.9}$$

The capacitance $c$ is related to the channel width $b$, as is $g$; $b$ in turn is related to the dc potential in the channel through the considerations of Chapter II which yield the relationship of $c$ and $g$ to $x$. This gives a linear differential equation with nonconstant coefficients for the product $gV$. In principle this equation can be solved; however, we find it more advantageous to attempt a useful approximation to this distributed case.

## C. A CIRCUIT MODEL BASED ON AN APPROXIMATION TO THE DISTRIBUTED LINE

From (3.6) we can construct one section of the line discussed above. At any point $x$ on the line

$$-i(x) = g \frac{dv}{dx} + \frac{dg}{dx} v$$

In a small region $\Delta x$ about $x$ we can replace the derivatives by differentials:

$$-i(x) = g(x) \frac{\Delta v}{\Delta x} + \frac{\Delta g}{\Delta x} v$$

This equation implies that the current in the section is the sum of a current proportional to the voltage across the section and a current proportional to the voltage at the end of the section. Equation (3.7) requires a capacitive element in shunt to account for the displacement current. One can then infer the lumped-element model of Fig. 7. We note that it is identical to the model of Fig. 3 with the exception that $R$ of Fig. 3 is not present.

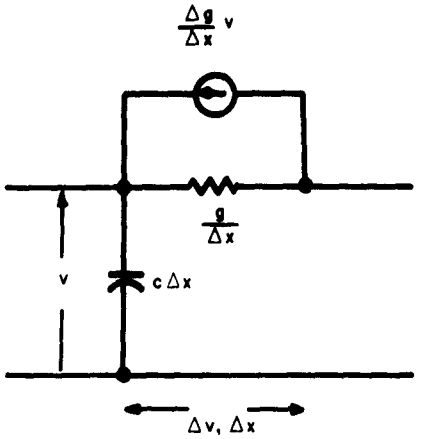



FIG. 7. A LUMPED-ELEMENT, ONE-SECTION MODEL FOR THE FET WAVE EQUATION.

Using the basic model of Fig. 7, we now derive a circuit model. A one-section line is inadequate to describe the device since it shows that the transconductance does not change with frequency and the input is purely capacitive (in a common source connection). Experiments have shown that this is not the case. If we cascade many sections the computation ease is lost and the efficacy of an approximation is removed. As a compromise a two-section model was chosen as the basis for subsequent calculations.

A two-section model is shown in Fig. 8. The sum of $\Delta x_1$ and $\Delta x_2$ is equal to the length of the channel, and the sum of the capacitances $C_1$, $C_2$, $C_3$ is equal to the total gate capacitance. The conductances must be distributed so as to match the dc solution. Before determining the actual size of the elements we can further simplify our model by making the following assumption:

$\Delta g_1/\Delta x_1$ is small; this is valid since the channel width varies slowly near the source [cf. Shockley, Ref. 1].

Using this assumption and letting

$$\frac{\Delta g_2}{\Delta x_2} = -G_T$$

$$\frac{g_2}{\Delta x_2} = \frac{1}{R_2}$$

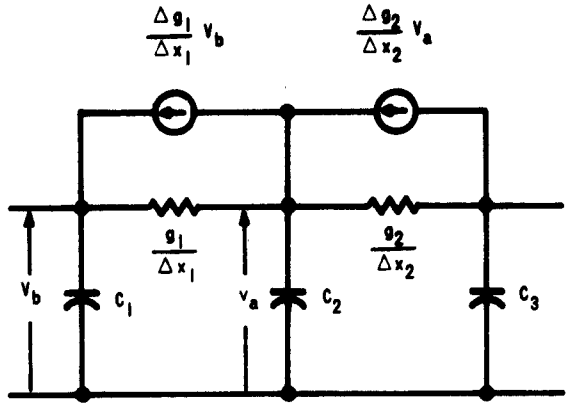



FIG. 8. A TWO-SECTION MODEL FOR THE FIELD-EFFECT TRANSISTOR.

$$\frac{g_1}{\Delta x_1} = \frac{1}{R_1}$$

we obtain the circuit model of Fig. 9.*

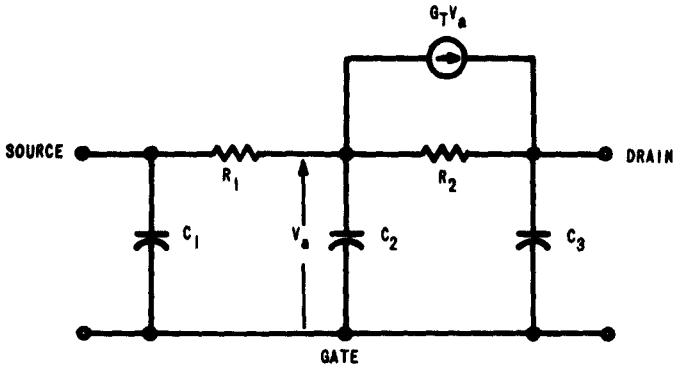
## D. CALCULATION OF THE ADMITTANCE PARAMETERS

The admittance parameters are defined by

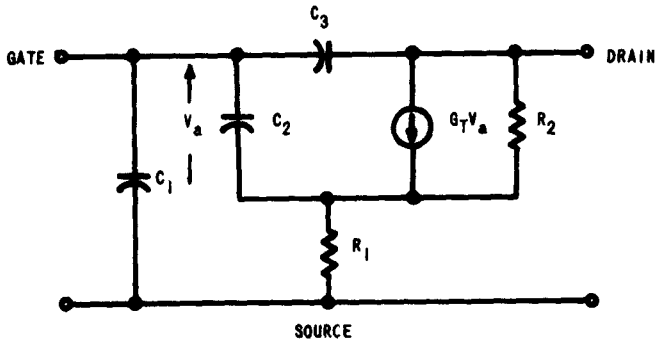
$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

*So far in this discussion we have neglected the effect of lead resistance and junction resistance on the circuit model. These may be included at this point. However, in well-designed devices, the gate junction resistance under reverse bias is small; hence, we shall neglect it at this point. Resistance in the source lead can be lumped with $R_1$; resistance in the drain lead cannot be lumped with $R_2$ due to the presence of the current generator $G_T V_a$. The series drain resistance could be added as an extrinsic resistance, but is neglected for the present.




a. Common gate




b. Common source ($V_a$ redefined in polarity)

FIG. 9. A CIRCUIT MODEL FOR THE FIELD-EFFECT TRANSISTOR.

and will be used to characterize the FET as a two-port network (cf. Fig. 10). The Y parameters are calculated for common-source connection. These are listed below in terms of the model of the preceding section:

$$Y_{11} = \frac{I_1}{V_1}\bigg|_{V_2=0} = j\omega(C_1 + C_3) + j\omega C_2 \left( \frac{1 + \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1} \right) \tag{3.10}$$

$$Y_{12} = \frac{I_1}{V_2}\bigg|_{V_1=0} = -j\omega C_3 \left( 1 + \frac{\frac{R_1 C_2}{R_2 C_3}}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1} \right) \tag{3.11}$$

$$Y_{21} = \frac{I_2}{V_1}\bigg|_{V_2=0} = G_T \left( \frac{1 - j\omega \frac{C_2 R_1}{G_T R_2}}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1} \right) \tag{3.12}$$

$$Y_{22} = \frac{I_2}{V_2}\bigg|_{V_1=0} = \frac{1}{R_2} \left( \frac{1 + j\omega C_2 R_1}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1} \right) \tag{3.13}$$

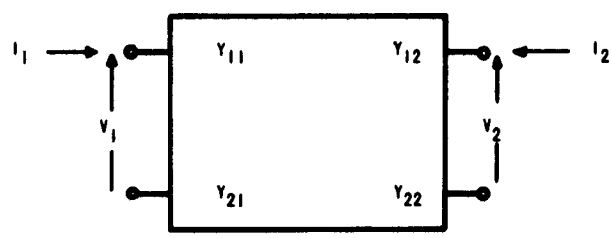



FIG. 10. A GENERAL TWO-PORT NETWORK CHARACTERIZED BY ADMITTANCE PARAMETERS.

At low frequencies the model should reduce to that calculated from the dc characteristics; i.e., in the common-source form, $Y_{21}$ should approach $G_m$, $Y_{22}$ should approach $G_d$, and $Y_{11}$ and $Y_{12}$ should become predominantly capacitive. For

$$\omega \ll \frac{1 + \frac{R_1}{R_2} + G_T R_1}{C_2 R_1}$$

(3.10) through (3.13) become

$$Y_{11} \cong j\omega(C_1 + C_3) + j\omega C_2 \left( \frac{1 + \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2} + G_T R_1} \right)$$

$$Y_{12} \cong -j\omega C_3 \left( 1 + \frac{\frac{R_1 C_2}{R_2 C_3}}{1 + \frac{R_1}{R_2} + G_T R_1} \right)$$

$$Y_{21} \cong \frac{G_T}{1 + \frac{R_1}{R_2} + G_T R_1}$$

$$Y_{22} \cong \frac{1}{R_2} \frac{1}{1 + \frac{R_1}{R_2} + G_T R_1}$$

For a match with the low-frequency calculations we require

$$G_m = \frac{G_T}{1 + \frac{R_1}{R_2} + G_T R_1}$$

$$G_d = \frac{1}{R_2} \frac{1}{1 + \frac{R_1}{R_2} + G_T R_1}$$

$$\mu = \frac{G_m}{G_d} = G_T R_2$$

From (2.13) one finds that

$$G_m + G_d = \frac{g_o}{L}\left[1 - \left(\frac{V_s - V_g}{W_o}\right)^{1/2}\right] \tag{3.14}$$

which is a constant with respect to the drain voltage. Let

$$G_m + G_d = G_{mo} \tag{3.15}$$

Then

$$G_{mo} = \frac{G_T + \frac{1}{R_2}}{1 + \frac{R_1}{R_2} + G_T R_1}$$

which yields

$$1 + \frac{R_1}{R_2} + G_T R_1 = \frac{1}{1 - G_{mo} R_1} \tag{3.16}$$

An important assumption is now made that simplifies computations. This assumption is to relate $R_1$ to the low-frequency parameters $G_m$ and $G_d$ through a constant as follows: divide the channel into two sections, letting the section nearer the source have a length $\lambda L$. Referring to Fig. 1, the resistance of this length of channel is, approximately,

$$R_1 \cong \frac{\lambda L}{\sigma_o B[b(0) + b(\lambda L)]}$$

If the channel width does not vary appreciably over the region from $x = 0$ to $x = \lambda L$, then

$$R_1 \cong \frac{\lambda L}{2\sigma_o B b(0)} \tag{3.17}$$

But

$$2\sigma_o \frac{B}{L} b(0) = 2\sigma_o \frac{B}{L} a\left[1 - \left(\frac{V_s - V_g}{W_o}\right)^{1/2}\right] \tag{3.18}$$

since the channel potential at $x = 0$ is $V_s - V_g$. Combining (3.14) and (3.17), we obtain

$$R_1 \cong \frac{\lambda}{G_m + G_d} = \frac{\lambda}{G_{mo}} \tag{3.19}$$

The quantity $\lambda$ is the fractional length of the section of the transmission line nearer the source. As the lumping procedure is an approximation only, $\lambda$ is obtained most easily by experimental means. The procedure used in the following work is to determine $\lambda$ from the input conductance at high frequencies.

The approximate value of $R_1$ is now used to calculate the admittance parameters. A cutoff frequency, $\omega_o$, is defined as

$$\omega_o \triangleq \frac{1 + \frac{R_1}{R_2} + G_T R_1}{C_2 R_1} \tag{3.20}$$

Utilizing (3.16) and (3.19), we can express (3.20) as

$$\omega_o = \frac{G_m + G_d}{(1 - \lambda)\lambda C_2} \tag{3.21}$$

Applying (3.19) and (3.20) to the admittance parameters, Eqs. (3.10) through (3.13), we obtain the following equations:

$$Y_{11} = j\omega \left[ C_1 + C_3 + \frac{C_2(1 - \lambda)}{1 + j\frac{\omega}{\omega_o}} \left( 1 + \frac{\lambda G_d}{(1 - \lambda)G_{mo}} \right) \right] \tag{3.22}$$

$$Y_{12} = -j\omega \left[ C_3 + \frac{\lambda C_2 \frac{G_d}{G_{mo}}}{1 + j\frac{\omega}{\omega_o}} \right] \tag{3.23}$$

$$Y_{21} = G_m \left[ \frac{1 - j\frac{\omega}{\omega_o}\frac{1}{(1 - \lambda)\mu}}{1 + j\frac{\omega}{\omega_o}} \right] - j\omega C_3 \tag{3.24}$$

$$Y_{22} = G_d \left[ \frac{1 + j \frac{\omega}{\omega_o} \frac{1}{1 - \lambda}}{1 + j \frac{\omega}{\omega_o}} \right] + j\omega C_3 \tag{3.25}$$

As the maximum transconductance occurs at pinch-off, one would more than likely operate the device at this point. Accordingly the assumption can be made that $\mu$ is large or, equivalently, that $G_d/G_m$ is less than one. Then the Y parameters are (separated into real and imaginary components):

$$Y_{11} = \frac{\frac{G_m}{\lambda} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2} + j\omega \left[ C_1 + C_3 + \frac{(1 - \lambda)C_2}{1 + \left(\frac{\omega}{\omega_o}\right)^2} \right] \tag{3.26}$$

$$Y_{12} = - \frac{(1 - \lambda)G_d \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2} - j\omega C_3 \tag{3.27}$$

$$Y_{21} = \frac{G_m}{1 + \left(\frac{\omega}{\omega_o}\right)^2} - j\omega \left[ \frac{\frac{G_m}{\omega_o}}{1 + \left(\frac{\omega}{\omega_o}\right)^2} + C_3 \right] \tag{3.28}$$

$$Y_{22} = G_d \left[ \frac{1 + \frac{1}{1 - \lambda} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2} \right] + j\omega C_3 \tag{3.29}$$

With the calculation of the admittance parameters, we have ostensibly completed the development of a circuit model. Several questions can now be asked: Is there a simpler representation, and What is the frequency limitation of the device? Both questions are answered in the following sections.

## E. A PI-SECTION REPRESENTATION

A pi-section model for the FET of the form shown in Fig. 11a, can be derived from the Y-parameter representation. For frequencies such that $\omega < \omega_o$ and if the voltage amplification factor $\mu$ is reasonably large, the preceding Y-parameter set (Eqs. 3.26 - 3.29) can be approximated by

$$Y_{11} \cong \frac{G_m}{\lambda} \left(\frac{\omega}{\omega_o}\right)^2 + j\omega(C_{gs} + C_{gd}) \tag{3.30}$$

$$Y_{12} \cong -j\omega C_{gd} \tag{3.31}$$

$$Y_{21} \cong \frac{G_m}{1 + j\frac{\omega}{\omega_o}} - j\omega C_{gd} \tag{3.32}$$

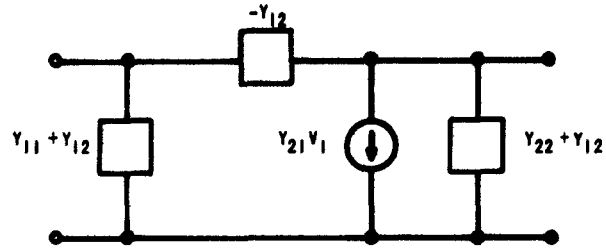
$$Y_{22} \cong G_d + j\omega C_{gd} \tag{3.33}$$

Substituting these parameters into the model of Fig. 11a results in the circuit of Fig. 11b. In addition the extrinsic drain resistance $r_d$, has been included for completeness. For low frequencies ($\omega << \omega_o$) the input conductance is negligible, the transconductance is constant, and the extrinsic drain resistance is negligible compared to the output resistance: in this case the circuit model simplifies to tnat of Fig. 11c.

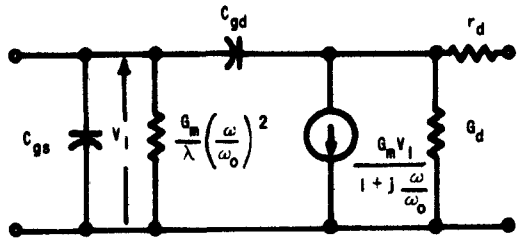
The model of Fig. 11b is similar to that often stated for the high-frequency circuit model of a vacuum tube [Ref. 8]. The input conductance due to transit-time loading in a vacuum tube is of the form

$$G_{in} = kG_m T^2 f^2$$

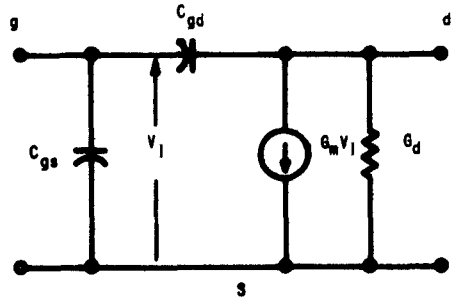
where $k$ is a constant (approximately 4), $G_m$ is the mutual conductance, $T$ is the grid-cathode transit time, and $f$ is frequency. In addition, the forward transadmittance becomes complex at high frequencies. This model is to be compared to the model shown in Fig. 11b.




a. General model




b. High-frequency model




c. Low-frequency model

FIG. 11. PI-SECTION REPRESENTATIONS OF THE FIELD-EFFECT TRANSISTOR.

## F. HIGH-FREQUENCY POWER GAIN AND THE MAXIMUM USEFUL FREQUENCY

Linvill and Gibbons [Ref. 9] have shown that the power gain of a two-port network defined by

$$PG = \frac{|Y_{21}|^2}{4Y_{11r}Y_{22r} - 2\mathcal{R}_e(Y_{12}Y_{21})} \tag{3.34}$$

is within 3 db of the maximum available gain (unless the device is potentially unstable at the frequency in question). The quantity PG is a useful measure of the performance of the device since it is independent of the terminations. The maximum useful frequency is defined as that frequency, $f_{max}$, at which PG is unity. This frequency is also the maximum frequency of oscillation of the device if PG is the maximum available gain. If PG is less than the maximum available gain, then the maximum frequency of oscillation is somewhat higher.

Using the pi-section model of Fig. 11b as the basis of the calculation,

$$PG = \frac{G_m^2 + \omega^2\left\{\frac{G_m}{\omega_o} + C_{gd}\left[1 + \left(\frac{\omega}{\omega_o}\right)^2\right]\right\}^2}{2\omega^2 C_{gd}\left[1 + \left(\frac{\omega}{\omega_o}\right)^2\right]\left\{\frac{G_m}{\omega_o} + C_{gd}\left[1 + \left(\frac{\omega}{\omega_o}\right)^2\right]\right\}} \tag{3.35}$$

Letting $\omega = \omega_{max}$ in (3.34) and PG = 1 we obtain the following equation:

$$\omega_{max}^2\left(\frac{C_{gd}}{G_m}\right)^2\left[1 + \left(\frac{\omega_{max}}{\omega_o}\right)^2\right] = 1$$

As $G_m/C_{gd}$ is about $\omega_o$,* an approximate solution to the above is

$$\omega_{max} \cong \omega_o \tag{3.36}$$

*From (3.21), $\omega_o = G_m/\lambda(1 - \lambda)C_2 = (G_m/C_{gd})(C_{gd}/\lambda(1 - \lambda)C_2)$. Since the gate capacitances are distributed so that $C_{gd}$ is less than $C_2$, the reduced capacitance $\lambda(1 - \lambda)C_2$ is about $C_{gd}$. It then follows that $\omega_o \cong G_m/C_{gd}$.

The maximum useful frequency is thus approximately the same frequency at which the transconductance falls to one-half of its low-frequency value.

For a unity-coupled FET oscillator, Dacey and Ross [Ref. 2] showed that the maximum frequency of oscillation was the point at which the transconductance of the model of Fig. 3 fell by 3 db. The transmission-line model indicates a somewhat higher frequency.

## G. COMPARISON OF THEORY AND EXPERIMENT

To test the validity of these results, especially the circuit model of Fig. 11b, admittance measurements were made on several field-effect transistors manufactured commercially. These units were Texas Instruments TIX691, Crystalonics C615, and Fairchild FSP400. All are silicon transistors, with the first having a p-type channel and a diffused gate junction and the latter two having n-type channels. The C615 transistor is constructed using an alloy technique; the FSP400 is a diffused unit.

Low-frequency (1 kc) admittance measurements were made, using a Wayne-Kerr Universal Bridge B221 and a Hewlett-Packard 302A Wave Analyzer as a small-signal source and detector. These measurements are shown in Figs. 12 through 17 for various bias conditions. These 1-f parameters follow generally the bias variation predicted by the dc theory of Shockley. The gate-to-source capacitance is essentially constant with respect to drain voltage variations. This constancy might be expected since there is little voltage drop across the gate-source junction at any time.

Other relevant data, such as pinch-off voltage, leakage currents, and extrinsic drain resistance, are shown in Table 1. The extrinsic drain resistance was measured by the technique of Dacey and Ross [Ref. 2] with some modifications: if current is passed between source and drain, the open-circuit gate voltage (measured from drain to gate) is equal to the voltage drop across the extrinsic drain resistance. Since there is no current flowing out of the gate, the gate must assume the potential of the channel at the drain edge of the gate. Thus the open-circuit gate voltage is equal to the voltage drop from the drain contact to the

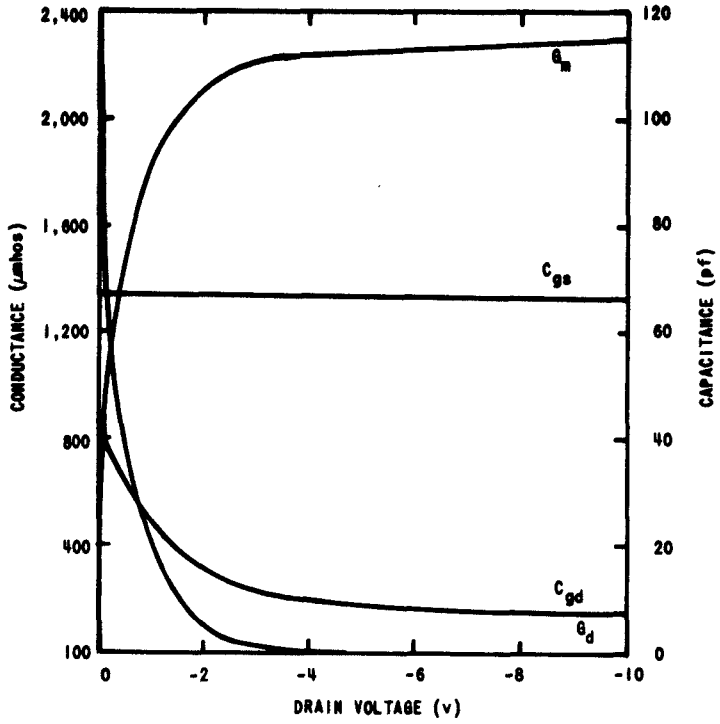



FIG. 12. LOW-FREQUENCY PARAMETERS FOR DEVICE TIX691 AS A FUNCTION OF DRAIN VOLTAGE (GATE VOLTAGE = 0 v).

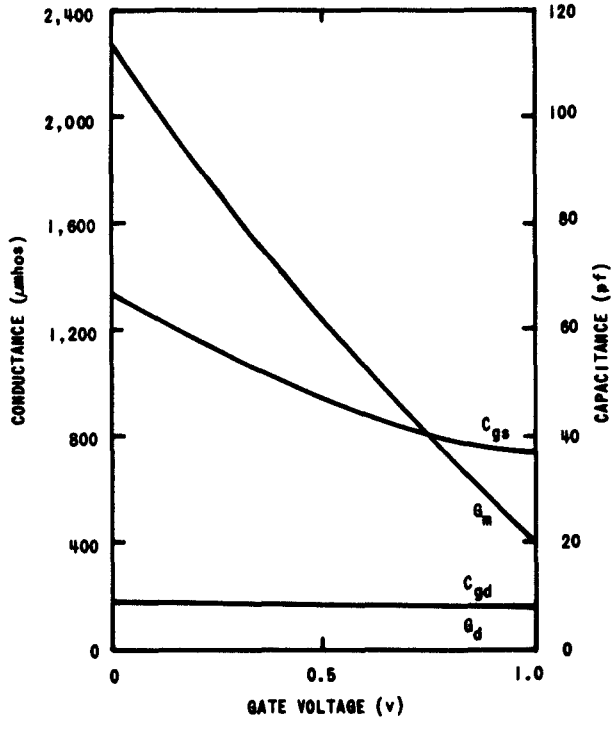



FIG. 13. LOW-FREQUENCY PARAMETERS FOR DEVICE TIX691 AS A FUNCTION OF GATE VOLTAGE (DRAIN VOLTAGE = -6 v).

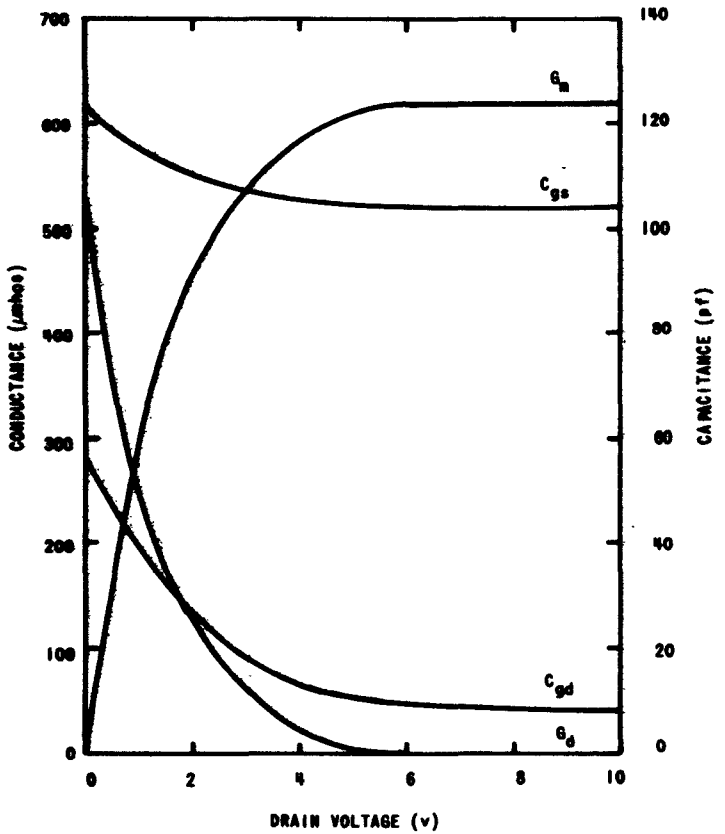



FIG. 14. LOW-FREQUENCY PARAMETERS FOR DEVICE C615 AS A FUNCTION OF DRAIN VOLTAGE (GATE VOLTAGE = 0 v).

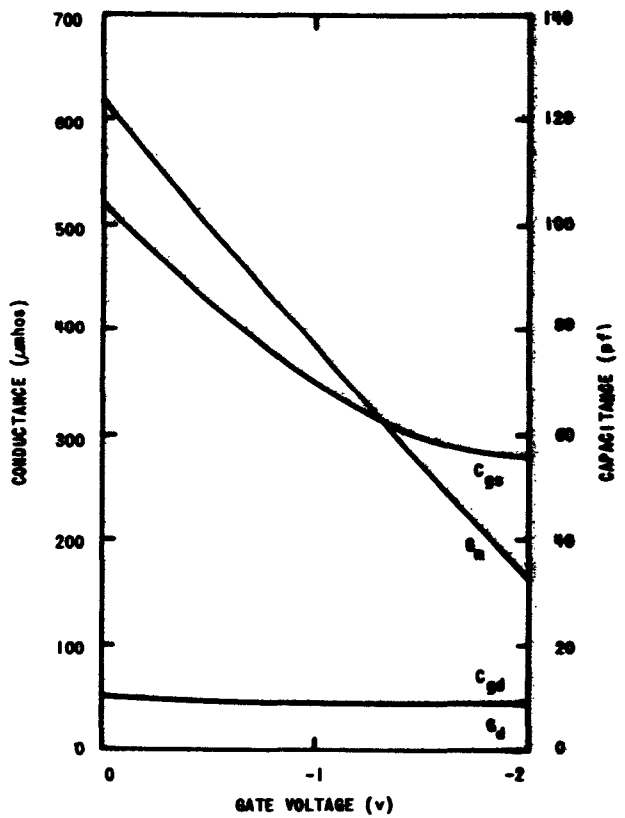



FIG. 15. LOW-FREQUENCY PARAMETERS FOR DEVICE C615 AS A FUNCTION OF GATE VOLTAGE (DRAIN VOLTAGE = 6 v).

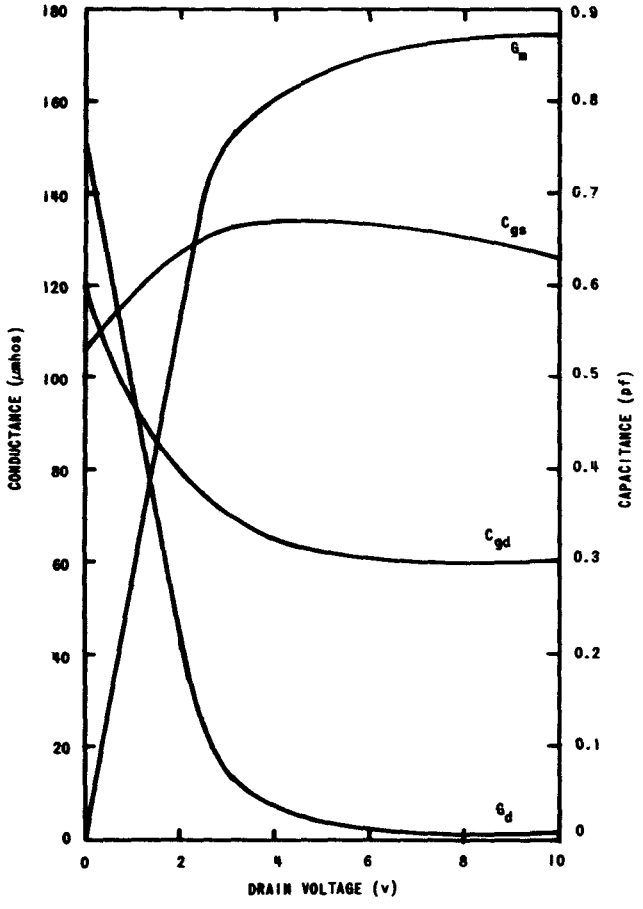



FIG. 16. LOW-FREQUENCY PARAMETERS FOR DEVICE FSP400 AS A FUNCTION OF DRAIN VOLTAGE (GATE VOLTAGE = 0 v).

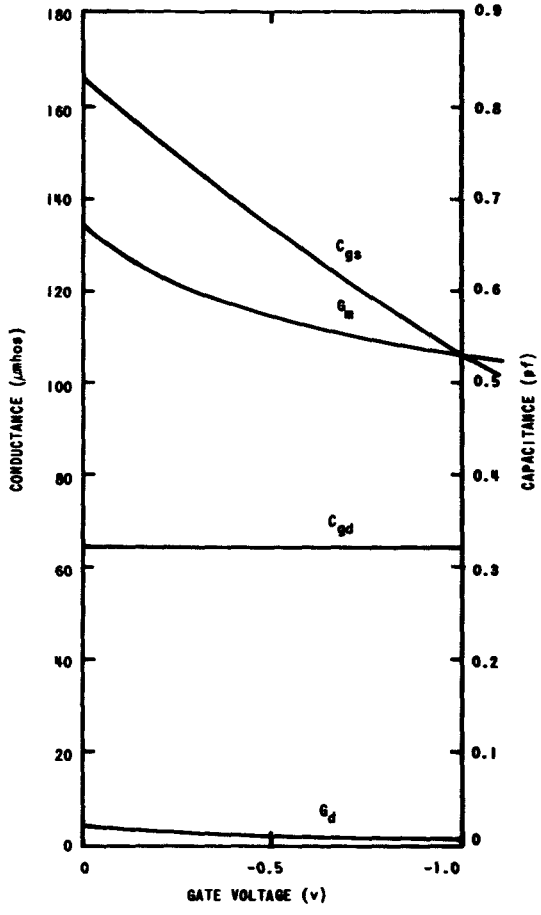



FIG. 17. LOW-FREQUENCY PARAMETERS FOR DEVICE FSP400 AS A FUNCTION OF GATE VOLTAGE (DRAIN VOLTAGE = 5 v).

TABLE 1. SOME LOW-FREQUENCY PARAMETERS

| Parameter | TIX691 | C615 | FSP400 |
|---|---|---|---|
| Pinch-off voltage $W_o$ | -4 v | 6 v | 5 v |
| Leakage current $V_d = W_o$, $V_g = 0$ | 2 na | 7 na | 0.1 na |
| $r_d$ | 57Ω | 320Ω | -- |

drain edge of the gate. The extrinsic drain resistance was obtained from the slope of the open-circuit gate voltage vs drain current curve. Using the slope, rather than the voltage divided by the current, eliminated any contact-potential problems.

To check the validity of the hf circuit model (Fig. 11b), admittance measurements were made for frequencies within the useful operating range of the devices. These measurements are depicted in Figs. 18 through 20. In the case of the TIX691 and the C615, the admittances were measured using a Wayne-Kerr B801 VHF Bridge, while the FSP400 admittances were measured using a General Radio 1607-A Transfer Function and Immittance Bridge. In the case of the imaginary parts of the admittances no attempts were made to separate the header capacitances or lead capacitances from the total capacitances. In the first two cases the capacitances were large enough to enable one to neglect any contribution from stray capacitances. In the case of the FSP400 the lead capacitances are probably not negligible in comparison with the extremely low internal capacitances of the device.

As mentioned previously, no attempt has been made in this theory to affix a theoretical value to $\lambda$ or to the "cutoff" frequency, $\omega_o$; but rather to set bounds on these numbers and describe the device from a circuit point of view. To determine the values of these hf parameters the following procedure was adopted: the frequency at which the forward transconductance fell to one-half of its l-f value was defined to be $\omega_o$, and $\lambda$ was determined at this same frequency from

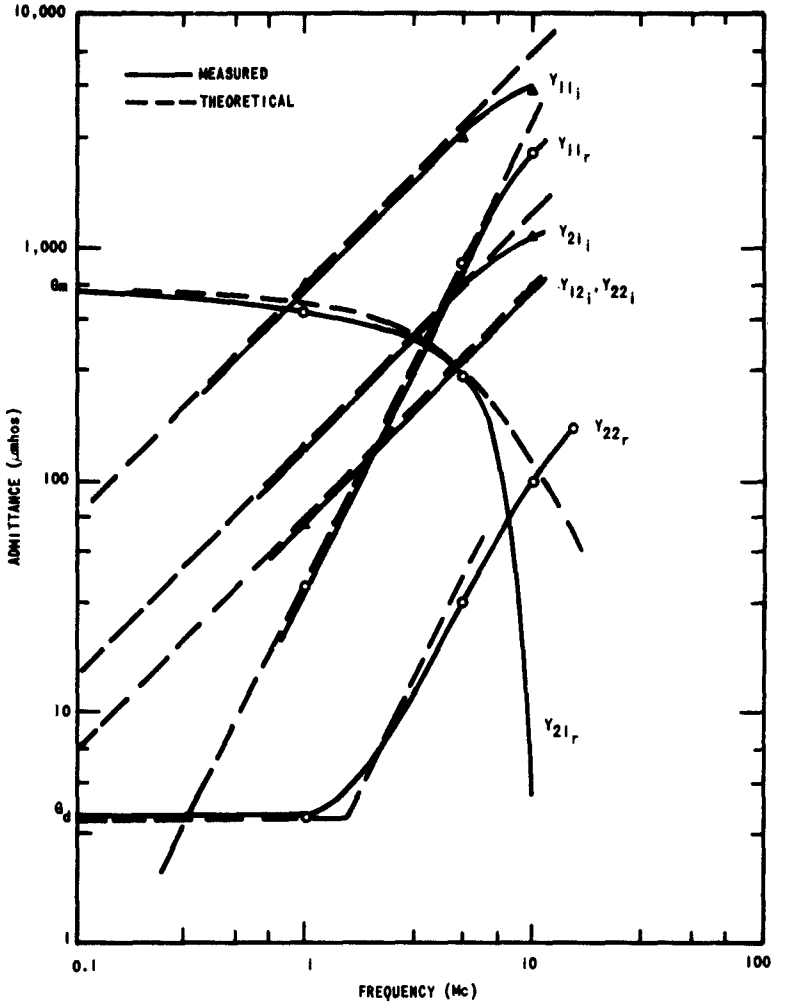



FIG. 18. HIGH-FREQUENCY Y PARAMETERS FOR DEVICE C615 ($V_d$ = 6 v, $V_g$ = 0 v).

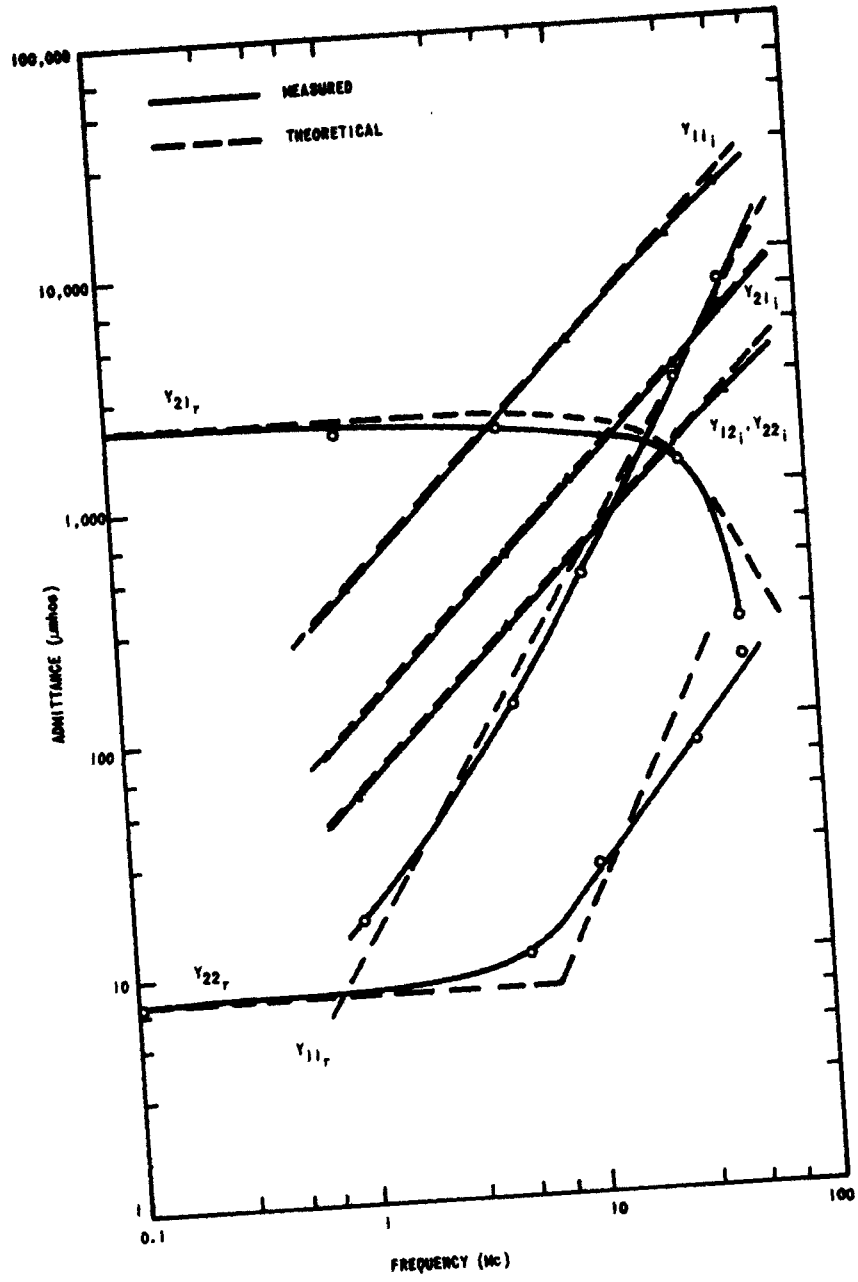



FIG. 19. Y PARAMETERS VS FREQUENCY FOR DEVICE TIX691 ($V_d$ = -6 v, $V_g$ = 0 v).

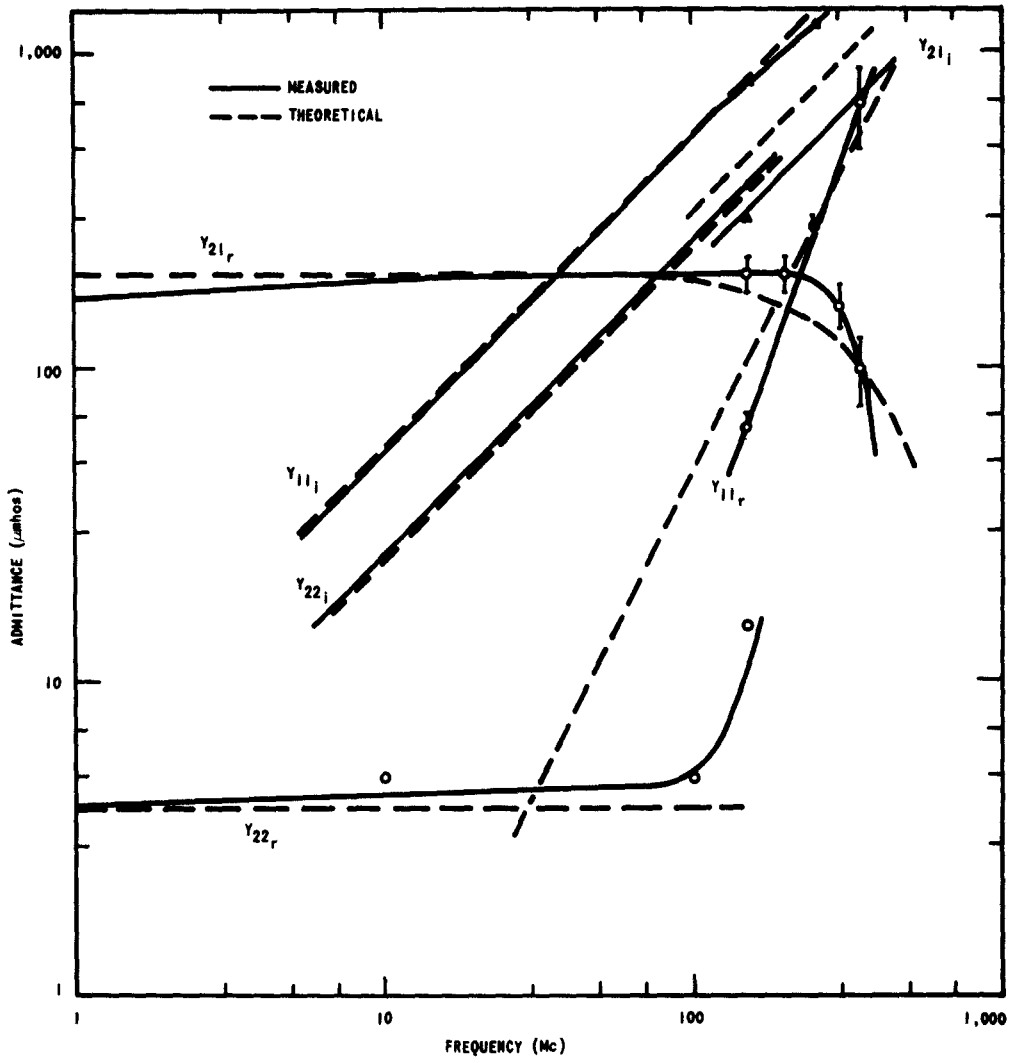



FIG. 20. Y PARAMETERS VS FREQUENCY FOR DEVICE FSP400 ($V_d$ = 5 v, $V_g$ = 0 v).

$$\lambda = \frac{G_m}{Y_{11r}(\omega_o)}$$

From these two parameters and the 1-f measurements, the theoretical curves were drawn (shown in dashed lines on the measured curves). The agreement is quite good for frequencies less than the cutoff frequency $\omega_o$.

The hf susceptances agree closely except in the case of FSP400. The forward transusceptance should be larger than the output susceptance by an amount proportional to the internal phase shift, $\omega G_m/\omega_o$. The measurements indicate that $Y_{22i}$ is larger than $Y_{21i}$.

In Table 2 the values of the hf parameters, $\lambda$ and $\omega_o$ are shown for the bias condition indicated. As can be seen, $\lambda$ varies widely from device to device, as does $\omega_o$. The behavior of $\lambda$ and $\omega_o$ is not, however, inconsistent with the previous considerations.

TABLE 2. HIGH-FREQUENCY PARAMETERS

| Device | $\lambda$ | $f_o = \frac{\omega_o}{2\pi}$ (Mc) |
|---|---|---|
| TIX691 $V_d = -6$ v, $V_g = 0$ | 0.57 | 35 |
| C615 $V_d = 6$ v, $V_g = 0$ | 0.87 | 4.6 |
| FSP400 $V_d = 5$ v, $V_g = 0$ | 0.28 | 350 |

The effect of drain voltage on cutoff frequency is shown in Fig. 21. From the transmission-line model the cutoff frequency $\omega_o$ is given by

$$\omega_o = \frac{G_{mo}}{\lambda(1-\lambda)C_2}$$

In the above equation all of the quantities, except $C_2$, are constant with respect to the drain voltage. The capacitance $C_2$ is the portion of the input capacitance that lies between the gate and the center of

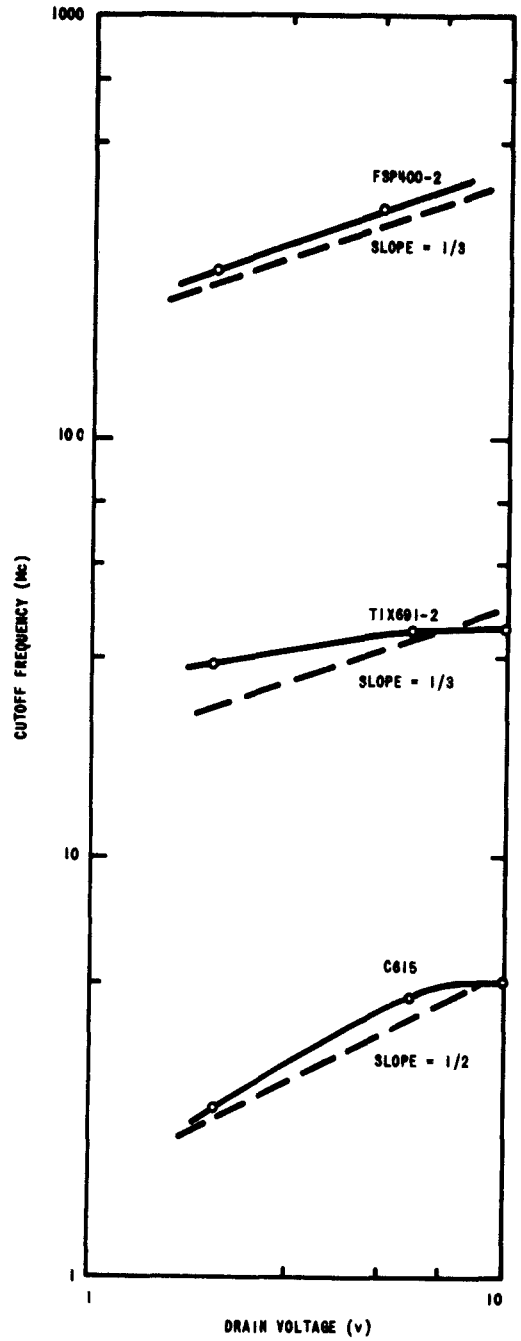



FIG. 21. MEASURED CUTOFF FREQUENCY VS DRAIN VOLTAGE FOR THE FIELD-EFFECT TRANSISTOR.

the channel. To a first approximation, $C_2$ varies as the drain voltage to the minus one-half or minus one-third power, corresponding to an abrupt gate junction or a graded gate junction, respectively. For reference purposes lines of the appropriate slope for the respective devices are drawn on Fig. 21. As can be seen, the measured values follow the indicated slopes quite closely.

To determine the maximum useful frequency of the device the measured admittance parameters were substituted into the formula for the maximum power gain (Eq. 3.34). The maximum power gains for the various devices are indicated in Fig. 22, with the frequency scale normalized with respect to $\omega_o$. In the case of devices C615 and TIX691 the maximum power gain fell to unity at about $\omega_o$ as predicted. For device FSP400 the maximum frequency was considerably lower than predicted. In this case parasitic elements that might account for the low $f_{max}$ may have been neglected.

## H. SUMMARY OF RESULTS

The principal result of this chapter has been to derive a circuit model of the field-effect transistor valid over the useful frequency range of the transistor. From a transmission line model the analysis proceeded to the conclusion that the device is adequately characterized by a pi-section model which is similar to that of the vacuum tube at high frequencies. The model is completely determined by 1-f parameters such as transconductance, output conductance, gate-source capacitance and gate drain capacitance, and two hf parameters: cutoff frequency and a constant relating to the input conductance.

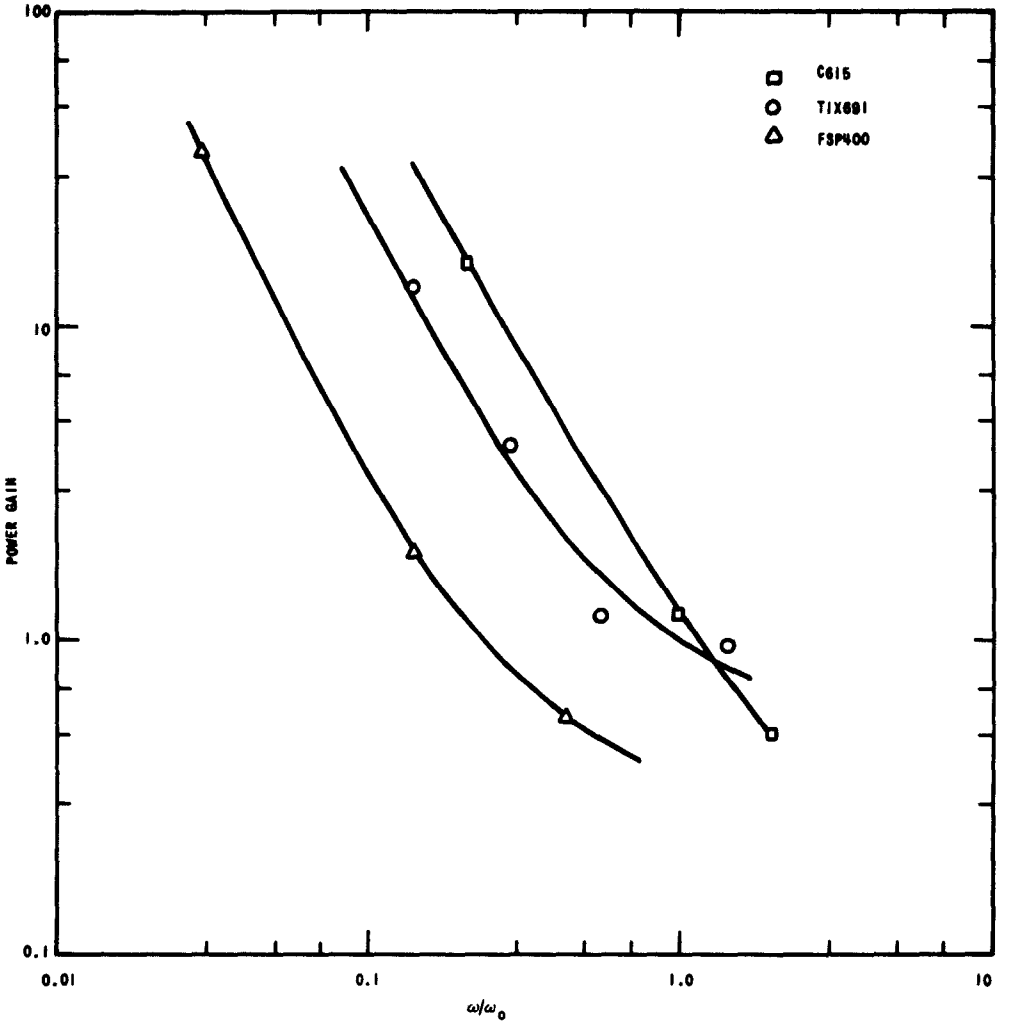



FIG. 22. MAXIMUM POWER GAIN VS NORMALIZED FREQUENCY.

## IV. THE NOISE MODEL

The derivation of the noise model begins with a postulation of noise-producing mechanisms. The mechanisms are characterized in the model by current and voltage sources. These internal sources are referred to the terminals of the devices as currents and the mean-square values of these terminal currents are computed. The terminal currents are used to compute the noise factor of the FET; the circuit and bias conditions that yield the minimum noise factor are determined. Measurements are made that indicate that the model is valid when 1/f noise is not important.

### A. NOISE-GENERATING MECHANISMS

Semiconductor noise can be classified into three classes: thermal noise, shot noise, and modulation noise. The first class is that associated with thermal agitation of carriers; the second arises from the discreteness of the carriers (their appearance and disappearance). Modulation noise is not well understood but appears to be caused by carrier fluctuations at the surface of the semiconductor. This noise is also called 1/f noise from the shape of its frequency spectrum.

Van der Ziel [Ref. 10] has suggested that the first class, thermal noise, be called diffusion noise, and the second class be called generation-recombination noise. Using these distinctions, the noise-producing mechanisms in semiconductor devices are more easily envisioned.

### B. CHANNEL NOISE

Current flow through the channel of the FET takes place by means of electrons and holes which drift under the influence of the electric field set up by the drain-source voltage. The noise associated with ohmic conduction is thermal noise. Thermal noise may be characterized by its mean-square fluctuation current, $\overline{i^2}$:

$$\overline{i^2} = 4kTG\Delta f \qquad (4.1)$$

where $k$ is Boltzmann's constant, $T$ is the absolute temperature, $G$ is the conductance of the noisy medium, and $\Delta f$ is the bandwidth of the observing instrument.*

This noise mechanism may be incorporated into a noise model of the FET by assigning thermal-noise generators of the form of (4.1) to the resistive elements of the transmission-line model of Fig. 8, viz. $R_1$ and $R_2$.** The generators are assumed to be uncorrelated.

Another source of noise in the channel is a density fluctuation caused by the generation and recombination of carriers. These density fluctuations produce, in turn, resistance fluctuations. The noise current associated with this phenomenon is proportional to the minority-carrier density in the channel since the fluctuation cannot exceed the average density of the smaller number of carriers (the minority carriers). For a typical field-effect transistor the doping of the channel material is such that the minority-carrier density is negligible compared to the majority-carrier density; thus this noise is negligible.

## C. GATE NOISE

The noise produced by the gate junction is the noise produced in a reverse-biased p-n junction or shot noise. Guggenbuehl and Strutt [Ref. 11] have shown that the mean-square noise current in a p-n junction diode is

$$\overline{i^2} = 4kTY_r\Delta f - 2qI\Delta f \qquad (4.2)$$

where $Y_r$ is the real part of the junction admittance, $q$ is the electronic charge, and $I$ is the current in the diode. This equation has been found to be invalid for silicon junctions where generation and recombination occur in the space-charge region [Ref. 12]. A more general expression for the p-n junction noise current is

---

*The spectrum of thermal noise is uniform up to infrared frequencies; thus, (4.1) is valid for all frequencies under consideration here.

**Van der Ziel has come to the same conclusion: the channel noise is primarily thermal noise [Ref. 3].

$$\overline{i^2} = 4kTY_r\Delta f - 2q\frac{I}{m}\Delta f \qquad (4.3)$$

where m is a parameter that depends on the mechanism of current flow, e.g., generation-recombination, and diffusion. This equation holds for all frequencies less than the transit-time limiting frequency for carriers crossing the junction.

For germanium junctions biased in the reverse direction the current flow is by means of diffusion: in this case m is one and $Y_r$ is zero. For silicon junctions the leakage current through the junction arises from generation in the space-charge region. As before, $Y_r$ is small, m is two. Since the devices under test are silicon units, we assume the latter conditions:

$$\overline{i^2} = q\, I_g \Delta f \qquad (4.4)$$

D. NOISE DUE TO LEAD RESISTANCE

Noise caused by resistance in the source and drain leads could be included in the model by assigning thermal-noise generators to these resistances. The generators would have the form

$$\overline{e^2} = 4kTr\,\Delta f \qquad (4.5)$$

where $\overline{e^2}$ is the mean-square voltage caused by the series resistance r. This noise is neglected in the following discussion since the noise contribution from the resistance is small.

E. THE NOISE MODEL

The noise-generating mechanisms are now incorporated into the transmission-line model of Fig. 9. In Fig. 23 noise generators are placed across each passive element of the transmission-line model. The generators are the Fourier transforms of the time-dependent random-noise currents. The generators $i_{n4}$ and $e_{n1}$ represent the thermal noise due to the resistance of the channel, while $i_{n1}$, $i_{n2}$, and $i_{n3}$ are the noise

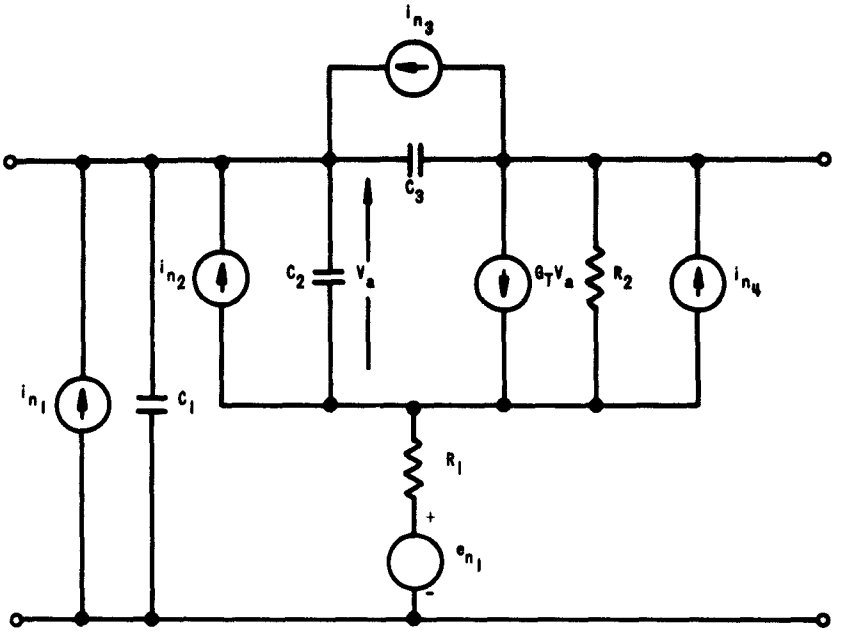



FIG. 23. NOISE MODEL BASED ON TRANSMISSION-LINE MODEL OF THE FIELD-EFFECT TRANSISTOR.

currents of the gate junction. The noise due to $R_1$ is represented as a voltage source for convenience only. The gate noise generators are distributed in the manner shown, since the gate current is distributed in the same way as the gate capacitances. All generators are assumed to be uncorrelated.*

To calculate the terminal noise currents, $I_{n1}$ and $I_{n2}$, defined in Fig. 24, the input and output terminals are shorted, and the short-circuit currents are calculated:

*Van der Ziel [Ref. 10] has discussed a possible modulation of the series resistance of a junction diode by the diode noise current. This would imply a correlation between the noise contribution of the series resistance and the noise contribution of the junction. In the case of the FET the series resistance is equivalent to the channel resistance and the diode is equivalent to the gate diode. He concludes, however, that this effect is negligible for small diode currents. Our assumption that there is no correlation between the channel noise generators and the gate noise generators is valid for a reverse-biased gate junction.


FIG. 24. SEPARATION OF NOISY FET INTO NOISELESS FET AND TWO TERMINAL NOISE CURRENTS.

$$I_{n1} = -i_{n1} - i_{n2}\left(1 - \frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}}\right) - i_{n3} + i_{n4}\left(\frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}}\right) - \frac{e_{n1}}{R_1}\left(\frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}}\right) \tag{4.6}$$

$$I_{n2} = \frac{\left(G_T + \frac{1}{R_2}\right) R_1 i_{n2}}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1} + i_{n3} - i_{n4}\left[1 - \frac{\left(G_T + \frac{1}{R_2}\right) R_1}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1}\right]$$

$$- e_{n1}\left[\frac{G_T + \frac{1}{R_2}}{1 + \frac{R_1}{R_2} + G_T R_1 + j\omega C_2 R_1}\right] \tag{4.7}$$

In terms of the 1-f parameters and the two hf parameters, these currents are

$$I_{n1} = - i_{n1} - \frac{i_{n2}}{1 + j\frac{\omega}{\omega_o}} - i_{n3} + i_{n4}\frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}} - \frac{e_{n1}}{R_1}\frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}} \tag{4.8}$$

$$I_{n2} = \frac{\lambda}{1 + j\frac{\omega}{\omega_o}} i_{n2} + i_{n3} + \frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}} i_{n4} - \frac{e_{n1}}{R_1}\frac{j\frac{\omega}{\omega_o}}{1 + j\frac{\omega}{\omega_o}} \tag{4.9}$$

The mean-square currents and their correlation are:

$$\overline{I_{n1}^2} = \overline{I_{n1}I_{n1}^*} = \overline{i_{n1}^2} + \frac{\overline{i_{n2}^2}}{1 + \left(\frac{\omega}{\omega_o}\right)^2} + \overline{i_{n3}^2} + \frac{\left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\overline{i_{n4}^2}$$

$$+ \frac{\left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\frac{\overline{e_{n1}^2}}{R_1^2} \qquad (4.10)$$

$$\overline{I_{n2}^2} = \overline{I_{n2}I_{n2}^*} = \frac{\lambda^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\overline{i_{n2}^2} + \overline{i_{n3}^2} + \left| 1 - \frac{\lambda}{1 + j\frac{\omega}{\omega_o}} \right|^2 \overline{i_{n4}^2}$$

$$+ \frac{(G_m + G_d)^2}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\overline{e_{n1}^2} \qquad (4.11)$$

$$\overline{I_{n1}^* I_{n2}} = -\overline{i_{n3}^2} - \frac{\lambda}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\overline{i_{n2}^2} + \left[\frac{j\frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\right]\left(1 - \lambda + j\frac{\omega}{\omega_o}\right)\overline{i_{n4}^2}$$

$$- \frac{\lambda j\frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{\omega_o}\right)^2}\frac{\overline{e_{n1}^2}}{R_1^2} \qquad (4.12)$$

where the * denotes complex conjugate. We assume the appropriate forms for the internal generators. The thermal-noise generators of the channel are

$$\overline{e_{n1}^2} = 4kTR_1\Delta f \qquad (4.13)$$

$$\overline{i_{n4}^2} = 4kT\frac{1}{R_2}\Delta f \qquad (4.14)$$

The shot-noise generators are distributed so that the total leakage current $I_g$ is equal to the sum of the distributed currents, $I_{g1}$, $I_{g2}$, and $I_{g3}$:

$$\overline{i_{n1}^2} = qI_{g1}\,\Delta f \tag{4.15}$$

$$\overline{i_{n2}^2} = qI_{g2}\,\Delta f \tag{4.16}$$

$$\overline{i_{n3}^2} = qI_{g3}\,\Delta f \tag{4.17}$$

The coefficients of the internal noise generators in (4.10), (4.11), and (4.12) are related to the admittance parameters of the FET through (3.10) through (3.13). The terminal noise currents per unit bandwidth become:

$$\overline{I_{n1}^2} = q\,I_{g1} + \frac{qI_{g2}}{1 + \left(\frac{\omega}{\omega_o}\right)^2} + qI_{g3} + 4kTY_{11r} \tag{4.18}$$

$$\overline{I_{n2}^2} = \frac{\lambda^2 qI_{g2}}{1 + \left(\frac{\omega}{\omega_o}\right)^2} + qI_{g3} + 4kTY_{22r} + 4kTY_{21r} \tag{4.19}$$

$$\overline{I_{n1}{}^{*}I_{n2}} = -\frac{\lambda qI_{g2}}{1 + \left(\frac{\omega}{\omega_o}\right)^2} - qI_{g3} + 4kTY_{12}{}^{*} + 4kTY_{21i} \tag{4.20}$$

assuming the internal generators are uncorrelated.

The above noise currents are valid over a frequency range which coincides with that of the circuit model. For $\omega \ll \omega_o$ the admittance parameters can be approximated by

$$Y_{11} \cong \frac{G_m + G_d}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2 + j\omega(C_{gs} + C_{gd}) \tag{4.21}$$

$$Y_{12} \cong -j\omega C_{gd} \tag{4.22}$$

$$Y_{21} \cong G_m - j\omega \left( \frac{G_m}{\omega_o} + C_{gd} \right) \tag{4.23}$$

$$Y_{22} \cong G_d + j\omega C_{gd} \tag{4.24}$$

Substituting these approximations into (4.18) through (4.20), the following noise currents are obtained:

$$\overline{I_{n1}^2} \cong qI_g + 4kT \frac{G_m + G_d}{\lambda} \left( \frac{\omega}{\omega_o} \right)^2 \tag{4.25}$$

$$\overline{I_{n2}^2} \cong \lambda^2 qI_{g2} + qI_{g3} + 4kT (G_d + \lambda G_m) \tag{4.26}$$

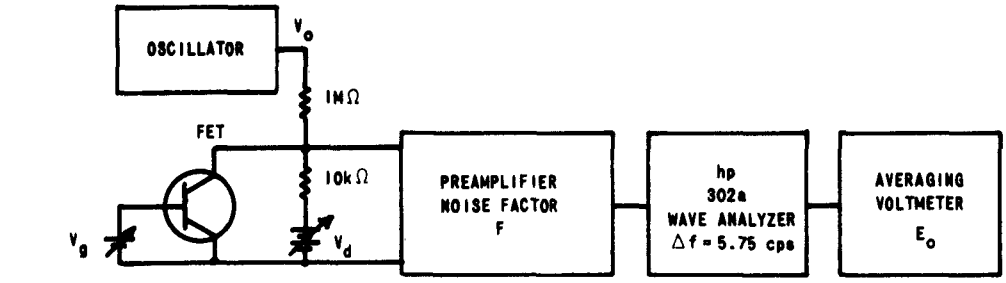
$$\overline{I_{n1} {}^* I_{n2}} \cong -\lambda qI_{g2} - qI_{g3} - 4kTj\omega \frac{G_m}{\omega_o} \tag{4.27}$$

These currents bear some similarity to their counterparts in vacuum tubes [Ref 13]. However, the noise is produced by a different mechanism. This similarity will be elaborated upon in the discussion of noise factor.

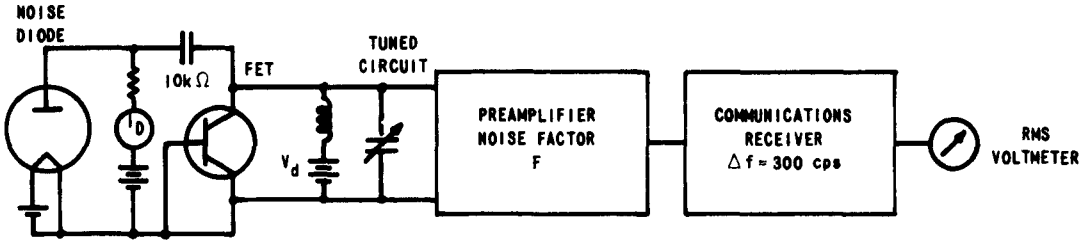
## F. NOISE-CURRENT MEASUREMENTS

To test the assumption that thermal noise is the primary source of noise in the channel, measurements of the output noise current $\overline{I_{n2}^2}$ were made on the FET's investigated previously. A frequency range that covered the 1-f spectrum from 100 cps to 50 kc was used, and both drain and gate voltages were varied. For one device, C615, hf measurements of the output noise current were made to test the validity of the theory near the cutoff frequency of the device. Block diagrams of the measuring apparatuses are shown in Fig. 25.

For the 1-f measurements the gain of the system, A, was measured using the oscillator as a source. Knowing the gain, the total noise at the output $\overline{E_o^2}$, the noise due to the 10-kilohm load resistance and the




a. Low frequency




b. High frequency

FIG. 25. MEASUREMENT OF FET OUTPUT NOISE CURRENT.

preamplifier noise factor F, the output noise current of the FET was calculated from

$$\overline{I_{n2}^2} = \frac{\overline{E_o^2}}{R_L^2 |A|^2} - F\,\overline{I_{nR_L}^2}$$

where

$$\overline{I_{nR_L}^2} = 4kT_o\,(1/R_L)\,\Delta f.^*$$

*This expression is correct if the total input resistance to the preamplifier is $R_L$, and if the noise factor of the preamplifier is measured with a source resistance of $R_L$.

The mean-square output noise voltage $\overline{E_o^2}$ was computed from the square-mean output voltage $(\overline{E}_o)^2$ by multiplying by 1.27.

For the hf measurement, a similar procedure was used except that a noise diode was the means of calibration. The output noise current from the FET was calculated from

$$\overline{I_{n2}^2} = 2q\, I_D\, \Delta f - F\, \overline{I_{nR}^2}$$

where $F\, \overline{I_{nR}^2}$ is the noise from the losses in the preamplifier input circuit but not including the FET output conductance, and $I_D$ is the noise diode current required to double the output noise power from the FET alone.

The results of these measurements are shown in Figs. 26 through 34 for various conditions of frequency, drain voltage, and gate voltage.* Measurements were made using drain voltages that maintained a large $\mu$.

Considering device C615 for example, Fig. 29 depicts the output noise current as a function of drain voltage for frequencies from 100 cps to 50 kc. The noise current increased for increasing drain voltage, approaching a constant for voltages beyond the pinch-off voltage. In addition, the noise current decreased for increasing frequency.

For comparison purposes a theoretical curve of the output noise current is also shown in Fig. 29. The current was calculated from (4.26), using the values of $G_d$, $G_m$, and $\lambda$ measured in Chapter III. The gate leakage current was neglected since the current was only several nanoamps for this device at the highest gate voltage used. The measured noise currents were larger than the theoretical current at all frequencies except 50 kc. Although the theoretical noise current remained essentially constant with drain voltage, the measured currents increased somewhat for drain voltages less than 6 v and were constant from 6 to 10 v.

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*The output noise current is plotted in terms of an equivalent noise current $I_{eq}$:

$$I_{eq} \triangleq \frac{\overline{I_{n2}^2}}{2q\Delta f}$$

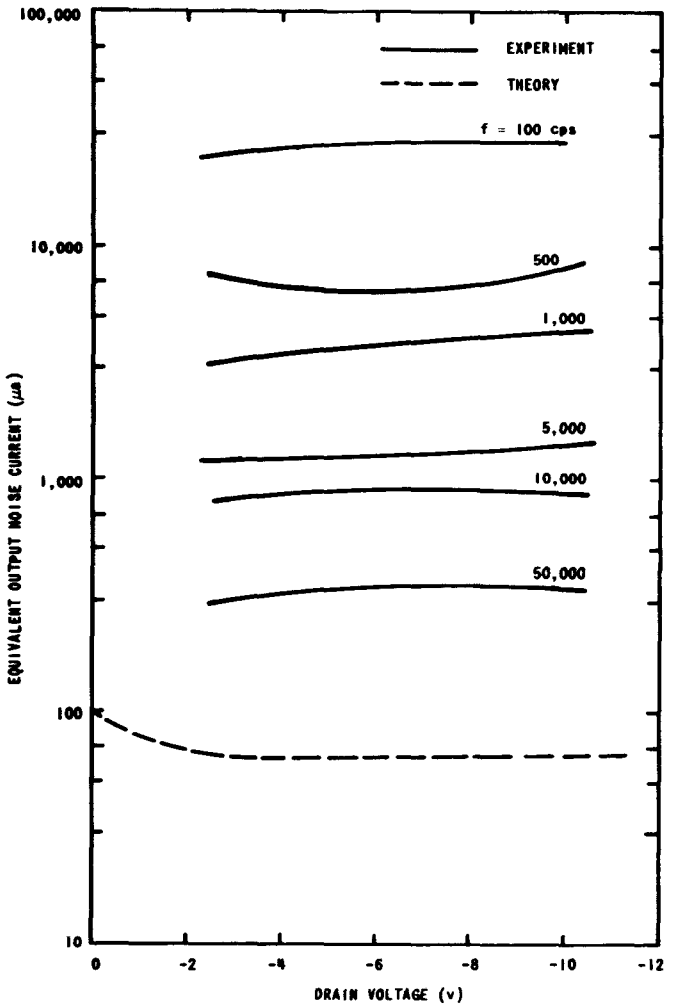


FIG. 26. OUTPUT NOISE CURRENT VS DRAIN VOLTAGE FOR DEVICE TIX691 WITH FREQUENCY AS A PARAMETER ($V_g$ = 0).

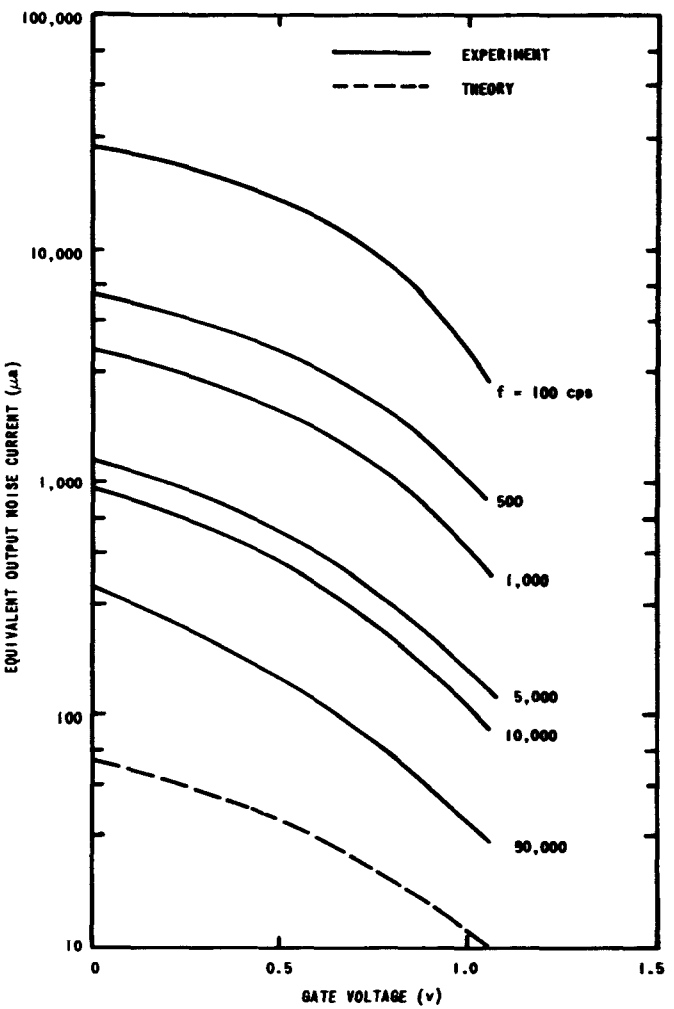


FIG. 27. OUTPUT NOISE CURRENT VS GATE VOLTAGE FOR DEVICE TIX691 WITH FREQUENCY AS A PARAMETER ($V_d$ = -6 v).

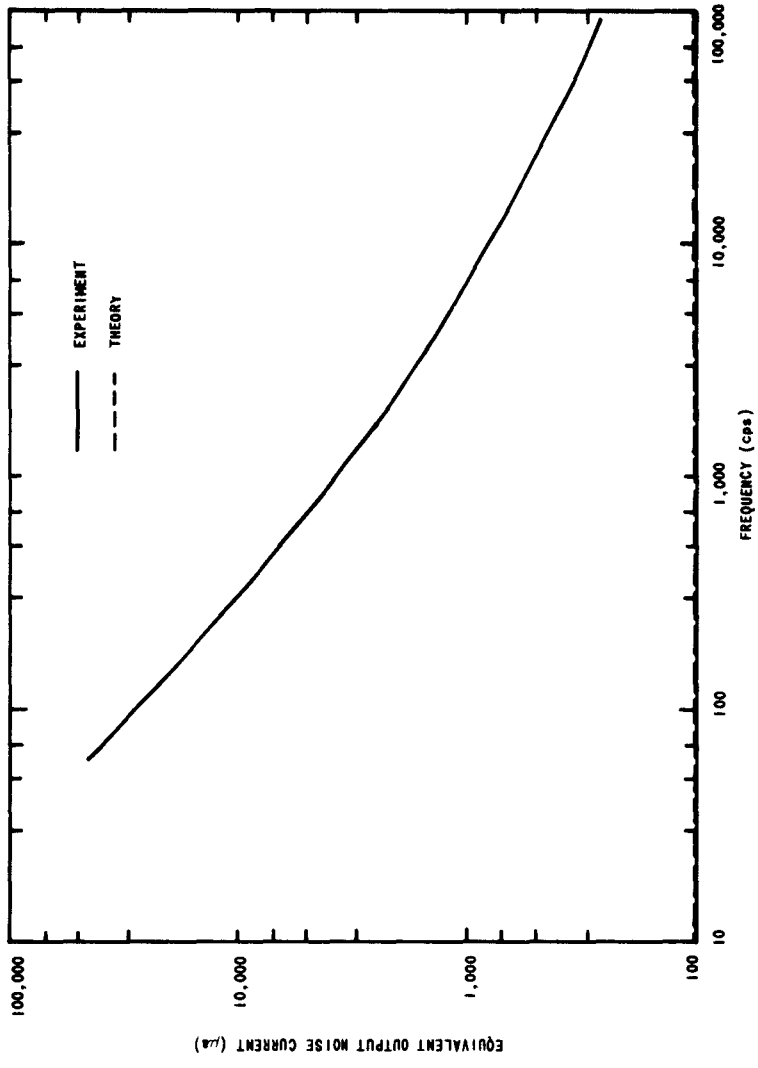


FIG. 28. OUTPUT NOISE CURRENT VS FREQUENCY FOR DEVICE TIX691 ($V_d$ = -6v).

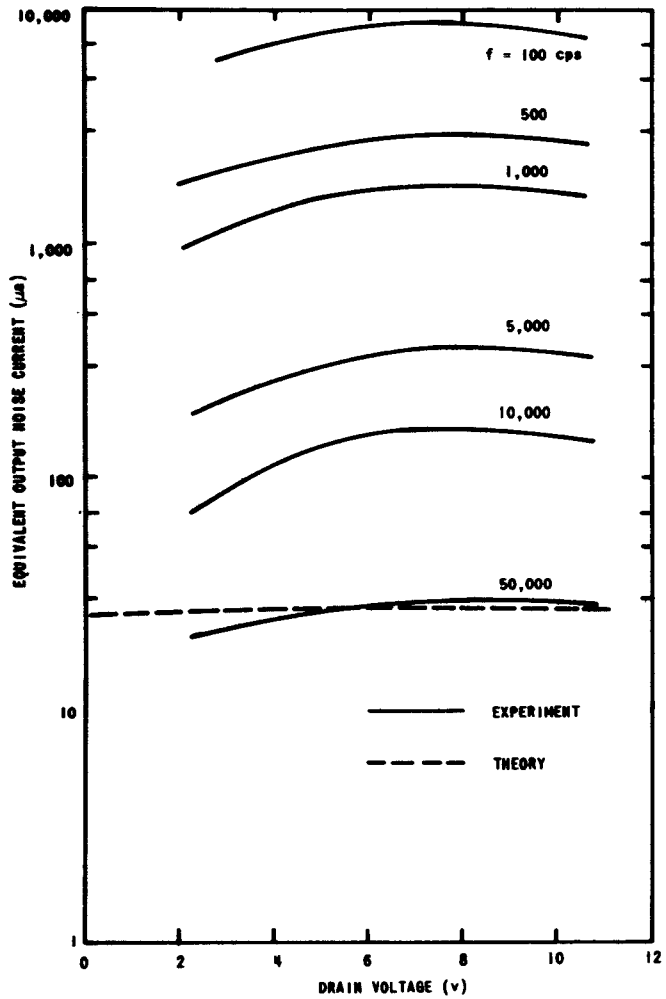


FIG. 29. OUTPUT NOISE CURRENT VS DRAIN VOLTAGE FOR DEVICE C615 WITH FREQUENCY AS A PARAMETER ($V_g$ = 0 v).

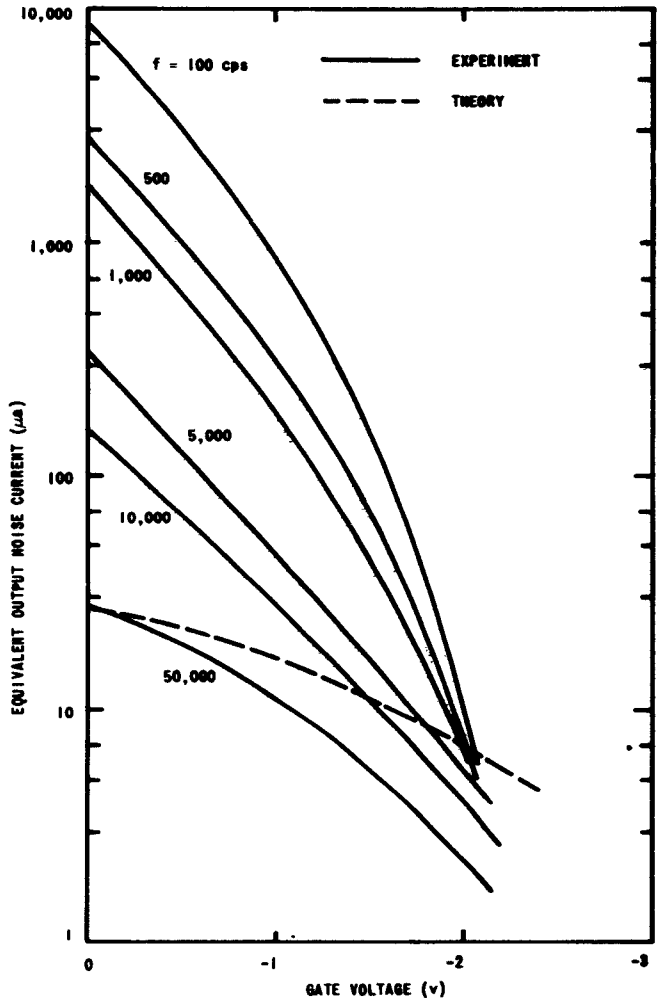


FIG. 30. OUTPUT NOISE CURRENT VS GATE VOLTAGE FOR DEVICE C615 WITH FREQUENCY AS A PARAMETER ($V_d$ = 6 v).

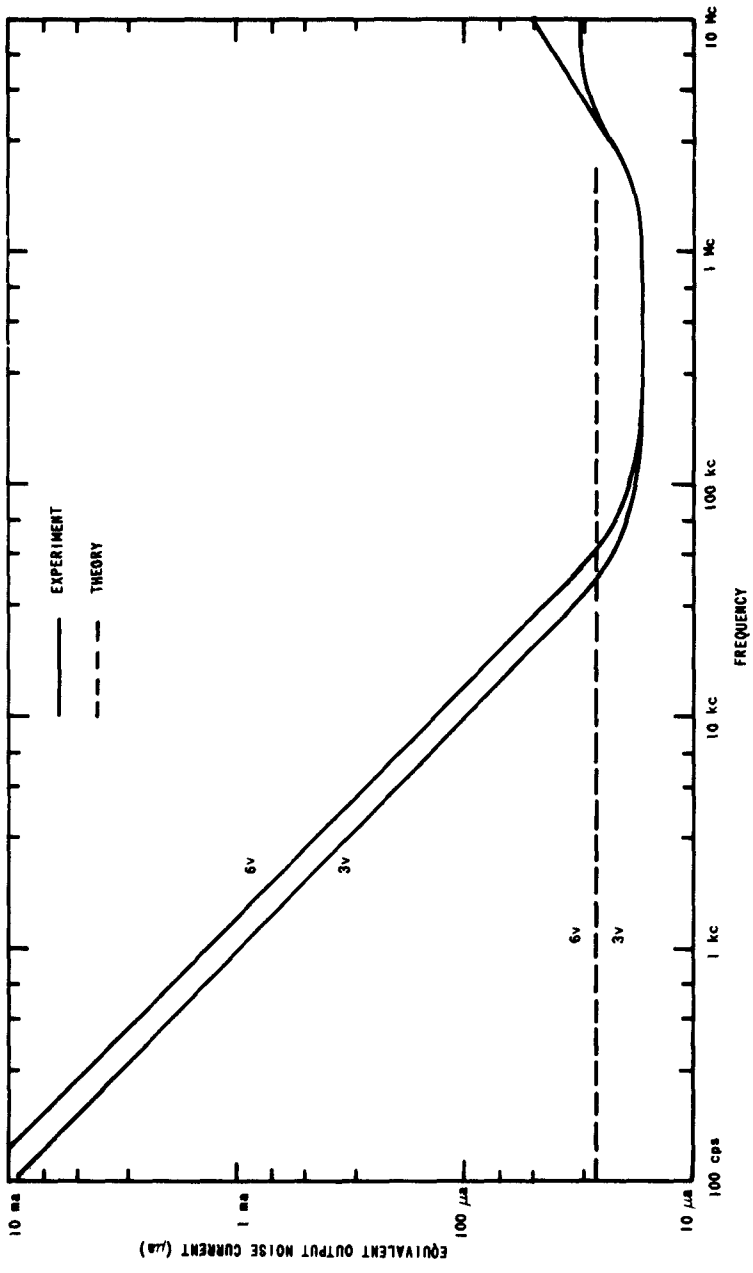


FIG. 31. OUTPUT NOISE CURRENT VS FREQUENCY FOR DEVICE C615 WITH DRAIN VOLTAGES OF 3 v AND 6 v ($V_g$ = 0 v).

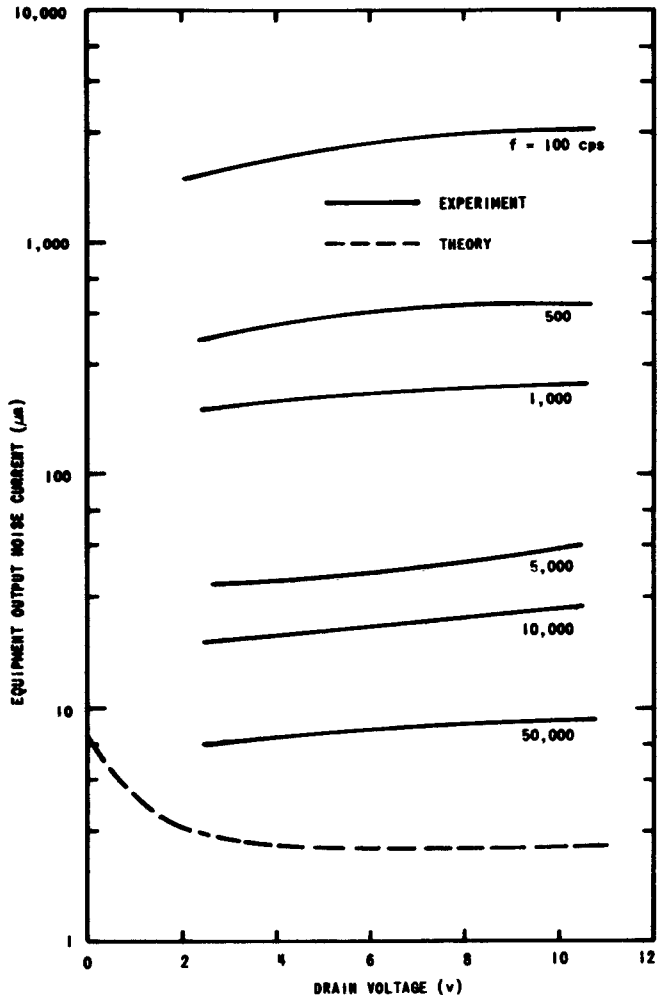


FIG. 32. OUTPUT NOISE CURRENT VS DRAIN VOLTAGE FOR DEVICE FSP400 WITH FREQUENCY AS A PARAMETER ($V_g$ = 0 v).

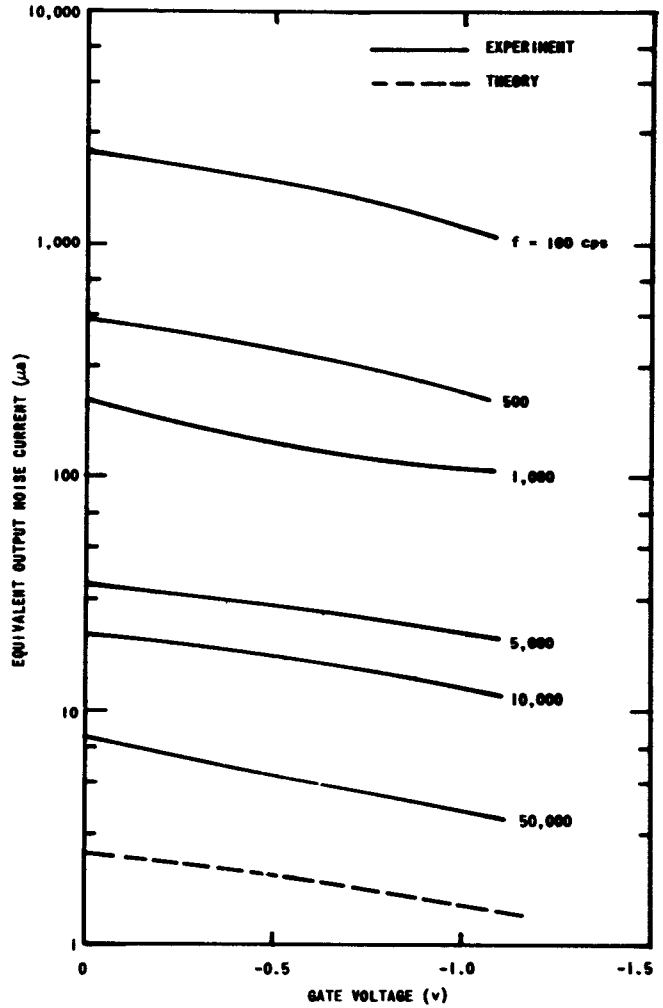


FIG. 33. OUTPUT NOISE CURRENT VS GATE VOLTAGE FOR DEVICE FSP400 WITH FREQUENCY AS A PARAMETER ($V_d$ = 5 v).

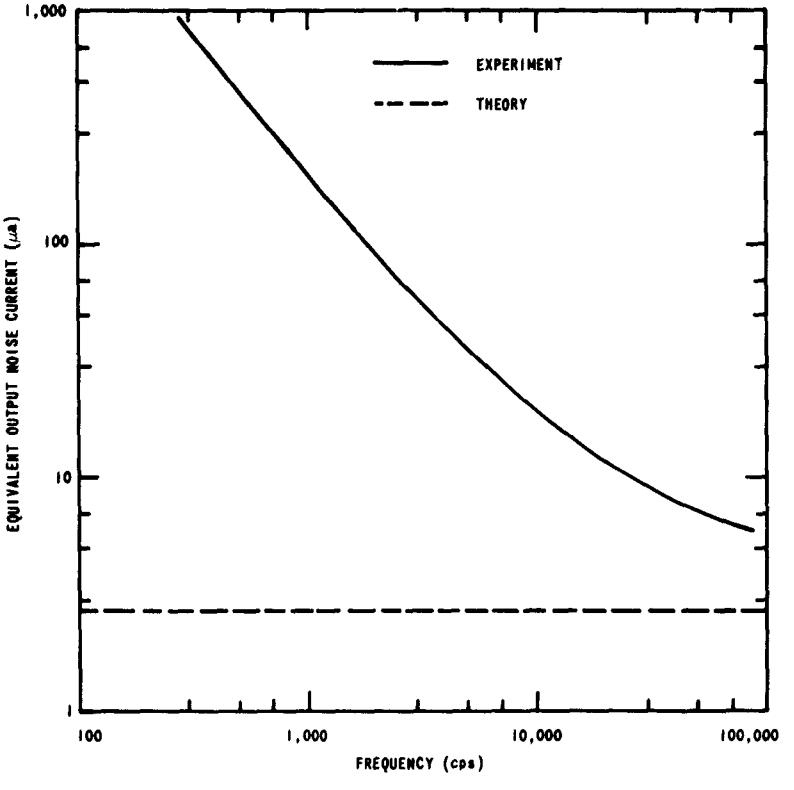


FIG. 34. OUTPUT NOISE CURRENT VS FREQUENCY FOR DEVICE FSP400 ($V_d$ = 5 v)

In Fig. 30 the output noise current is shown as a function of the gate voltage for a drain voltage of 6 v. As in Fig. 29 the noise current decreased as the frequency of measurement was increased and as the gate voltage was increased. The measured noise currents were again larger than the theoretical current.

A plot of the frequency spectrum is shown in Fig. 31 for several drain voltages. At low frequencies the spectrum has a slope of -1, characteristic of that class of low-frequency noise called 1/f noise. Above 50 kc the noise current becomes constant, until the cutoff frequency (5 Mc) is approached. At this point the noise increases due to the increase of $Y_{22r}$ (although the model is not necessarily valid at these frequencies).

We conclude from these measurements on C615 that thermal noise is the predominant noise mechanism at high frequencies, but that 1/f noise dominates at low frequencies.

Similar behavior of the noise current as a function of frequency is exhibited by the other devices tested, TIX691 and FSP400. The most conspicuous difference was the presence of excess noise at 50 kc in the latter two devices.

## G. THE NOISE FACTOR OF THE FET

The commonly accepted measure of the noise performance of a device is its noise factor. The noise factor F is defined by the relation

$$F = \frac{\text{noise power available at output}}{\text{noise power available at output due to the source alone}} \tag{4.28}$$

Using the representation of Fig. 24, the noise factor of the FET is

$$F = 1 + \frac{\overline{\left| I_{n1} - \frac{Y_{11}}{Y_{21}} I_{n2} - Y_s \frac{I_{n2}}{Y_{21}} \right|^2}}{4kT_o G_s \Delta f} \tag{4.29}$$

where $Y_s$ is the source admittance, and $4kT_o G_s \Delta f$ is the noise due to the source conductance $G_s$ at the reference temperature $T_o$.

The noise-factor formulation derived in the appendix is convenient for purposes of analysis. Using this formulation, the noise factor of any linear twoport is

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[(G_s + G_\gamma)^2 + (B_s + B_\gamma)^2\right] \tag{4.30}$$

where $G_u \triangleq$ the equivalent noise conductance

$R_n \triangleq$ the equivalent noise resistance

$G_\gamma \triangleq$ the correlation conductance

$B_\gamma \triangleq$ the correlation susceptance

In most instances the device will not be used at frequencies near cutoff, and the device will be operated near maximum gain. These two conditions imply $\omega \ll \omega_o$ and $G_d/G_m \ll 1$. The leakage conductance of the gate is small compared to the conductance of the channel; therefore the gate noise is small compared to the channel noise, or $qI_g/4kT_o\lambda G_m \ll 1$. The noise currents can then be approximated by

$$\overline{I_{n1}^2} \cong qI_g\Delta f + 4kT_o\frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2\Delta f \tag{4.31}$$

$$\overline{I_{n2}^2} \cong 4kT_o\,\lambda\,G_m\,\Delta f \tag{4.32}$$

$$\overline{I_{n1}{}^{*}I_{n2}} \cong -\lambda qI_{g2} - \lambda I_{g3} - 4kT_o j\omega\frac{G_m}{\omega_o} \tag{4.33}$$

The approximate admittance parameters [Eqs. (4.21) through (4.24)] are used in (A.14) through (A.18) in the appendix; the following equations result from this substitution:

$$R_n = \frac{\lambda}{G_m} \tag{4.34}$$

$$G_\gamma = \frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2 \tag{4.35}$$

$$B_\gamma = \omega(C_{gs} + C_{gd}) \tag{4.36}$$

$$G_u = \frac{qI_g}{4kT_o} - 2\frac{\omega^2}{\omega_o}(C_{gs} + C_{gd}) \tag{4.37}$$

The noise factor is computed from (4.30):

$$F = 1 + \frac{\frac{qI_g}{4kT_o} - 2\frac{\omega^2}{\omega_o}(C_{gs} + C_{gd})}{G_s} + \frac{\lambda}{G_m G_s}\left\{\left[G_s + \frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2\right]^2 + [B_s + \omega(C_{gs} + C_{gd})]^2\right\} \tag{4.38}$$

The noise factor can be minimized by choosing $G_s$ and $B_s$ properly: the source conductance for the minimum noise factor is

$$G_o = \frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2\left[1 + \frac{qI_g}{4kT_o}\frac{\lambda}{G_m}\left(\frac{\omega_o}{\omega}\right)^4 - \frac{2\omega_o(C_{gs} + C_{gd})}{\frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2}\right] \tag{4.39}$$

and the optimum source susceptance is

$$B_o = -\omega(C_{gs} + C_{gd}) \tag{4.40}$$

The value of the optimum noise factor is

$$F_o = 1 + 2\left(\frac{\omega}{\omega_o}\right)^2 + 2\frac{\lambda}{G_m}G_o \tag{4.41}$$

At low frequencies the source susceptance may be made zero for sake of simplicity. In this case the noise factor

$$F = 1 + \frac{\frac{qI_g}{4kT_o} - \frac{2\omega^2}{\omega}(C_{gs} + C_{gd}) + \frac{\lambda}{G_m}\omega^2(C_{gs} + C_{gd})^2}{G_s} + \frac{\lambda}{G_m G_s}\left[G_s + \frac{G_m}{\lambda}\left(\frac{\omega}{\omega_o}\right)^2\right]^2 \tag{4.42}$$

The optimum source conductance for this case is

$$G_o = \left[\frac{qI_g G_m}{\lambda 4kT_o} - \frac{2\omega^2}{\omega_o}(C_{gs} + C_{gd})\frac{G_m}{\lambda} + \left(\frac{G_m}{\lambda}\right)^2\left(\frac{\omega}{\omega_o}\right)^4 + \omega^2(C_{gs} + C_{gd})^2\right]^{1/2} \tag{4.43}$$

and the optimum noise factor is

$$F_o = 1 + 2\left(\frac{\omega}{\omega_o}\right)^2 + 2R_n G_o \tag{4.44}$$

where $G_o$ is defined by (4.43). At low frequencies the input conductance can be neglected in comparison to the input susceptance; in addition, the leakage currents are small. If these terms are neglected in (4.43), the optimum source conductance is

$$G_o \cong \omega(C_{gs} + C_{gd})\left[1 - \frac{2\frac{G_m}{\omega_o}}{\lambda(C_{gs} + C_{gd})}\right]^{1/2} \tag{4.45}$$

and the optimum noise factor is

$$F_o \cong 1 + 2R_n G_o \tag{4.46}$$

The optimum noise factor calculated previously is that obtained by optimizing the source resistance only. The noise factor can be minimized by a judicious choice of bias condition. Approximating

$$R_n \cong \frac{\lambda}{G_m}$$

$$G_o \cong \omega(C_{gs} + C_{gd})$$

the optimum noise factor, obtained by optimizing $G_s$, is

$$F_o = 1 + 2\frac{\lambda}{G_m}\omega(C_{gs} + C_{gd})$$

As the drain bias (with constant gate bias) is increased, the transconductance increases until pinch-off is reached; similarly the input capacitance decreases with increasing drain bias until pinch-off is reached. Hence, the minimum of $F_o$ is reached with the drain voltage at pinch-off. If the drain voltage is fixed and the gate voltage is increased, the transconductance decreases as does the input capacitance. The proper choice of gate voltage is not clear in this case. An approximate answer can be obtained by recognizing that the transconductance decreases more rapidly than does the input capacitance. Hence, the term $2(\lambda/G_m)\omega(C_{gs} + C_{gd})$ gets larger as the gate voltage gets larger. Thus, the gate voltage should be made as small as possible.

If the preceding results are examined closely, one observes that, in the case of a general source admittance $Y_s$, the optimum source admittance is, approximately, $Y_{11}^*$ if the equivalent noise conductance, $G_u$, is neglected. For $Y_s = G_s$ the optimum source conductance is about $|Y_{11}|$. In both cases the result of choosing a source admittance is to optimize the power transfer from the source. In most cases, however, $G_u$ cannot be neglected and the source conductance must be somewhat larger than predicted by the simple argument above.

If the source conductance is large compared to the input admittance of the FET, the noise factor is, approximately,

$$F = 1 + \frac{\lambda}{G_m} G_s \qquad (4.47)$$

This condition is often met for devices which have small input capacitances and for operation at low frequencies. A similar form for the noise factor of vacuum tube amplifiers is often stated. Moreover, the equivalent noise resistance $\lambda/G_m$ is similar to that of the vacuum tube [Ref. 13]. For

vacuum triodes the constant $\lambda$ is about 2.5; for the FET, $\lambda$ is less than 1. Thus the FET should have a smaller noise factor than a vacuum tube with the same transconductance and source conductance.

## H. NOISE-FACTOR MEASUREMENTS

Noise-factor measurements were made on the devices previously investigated using the test setup of Fig. 35. The results of varying source resistance, bias voltage, and frequency are shown in Figs. 36 through 41.

From a qualitative viewpoint the devices followed the theory in two respects: first, the optimum source conductance increased with frequency; and second, for the higher frequencies, the lowest noise factors were obtained for the device biased in the maximum gain condition, i.e., for the drain biased at pinch-off and the gate biased at zero volts. As would be expected by the implications of the preceding measurement of the output noise current, the noise factor increased as the frequency decreased due to 1/f noise effects.

To test the model, noise-factor measurements at 50 kc were used to compare with the predicted performance of device C615. As noted previously, this device showed little 1/f noise at this frequency. From the data the optimum noise factor, equivalent noise resistance, and optimum source resistance were determined. In Figs. 42 through 47 the measured and predicted values are depicted. The theoretical values were calculated from

$$R_n = \frac{1}{G_m}\left( \frac{G_d}{G_m} + \lambda \right) \tag{4.48}$$

$$R_o = \frac{1}{\omega(C_{gs} + C_{gd}) \left[ 1 - \frac{2G_m}{\lambda\omega_o(C_{gs} + C_{gd})} \right]^{1/2}} \tag{4.49}$$

$$F_o = 1 + 2R_n/R_o \tag{4.50}$$

The input resistance was neglected, as was the leakage current.

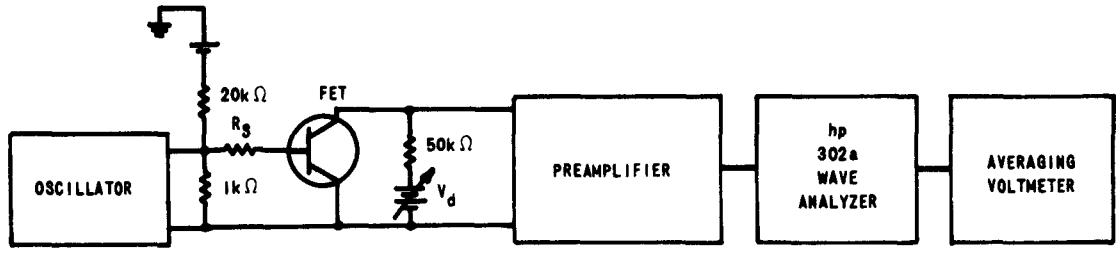


FIG. 35. TEST SETUP FOR MEASURING NOISE FACTOR.

As indicated by Figs. 37 and 38, the theoretical values of noise resistance compared closely with the measured values. However, the optimum noise factor as measured was higher than predicted by the theory of the preceding section. Also, the optimum source resistance was lower than predicted. Both of these deviations could be explained by 1/f noise in the input circuit. For example, if a 1/f noise current $\overline{I_{fl}^2}$ is added to the input noise current $\overline{I_{nl}^2}$, the new optimum source conductance, $G_o'$, becomes:

$$G_o' = \left[ \frac{qI_g G_m}{\lambda kT_o} + \frac{\overline{I_{fl}^2}\, G_m}{\lambda 4kT_o \Delta f} + \omega^2 (C_{gs} + C_{gd})^2 - 2 \frac{\omega^2}{\omega_o} \frac{G_m}{\lambda} (C_{gs} + C_{gd}) \right]^{1/2}$$

Thus a larger input noise current causes a larger optimum source conductance or a smaller source resistance. A larger optimum conductance results in an increased minimum noise factor through the relationship of (4.44). This input circuit noise is probably caused by a 1/f noise component in the gate leakage current, which often contains such a noise spectrum.

We conclude from these measurements on device C615 that thermal noise in the channel seemed to be the dominant noise at 50 kc; on the other hand, some excess noise was apparent at the input terminals at 50 kc.

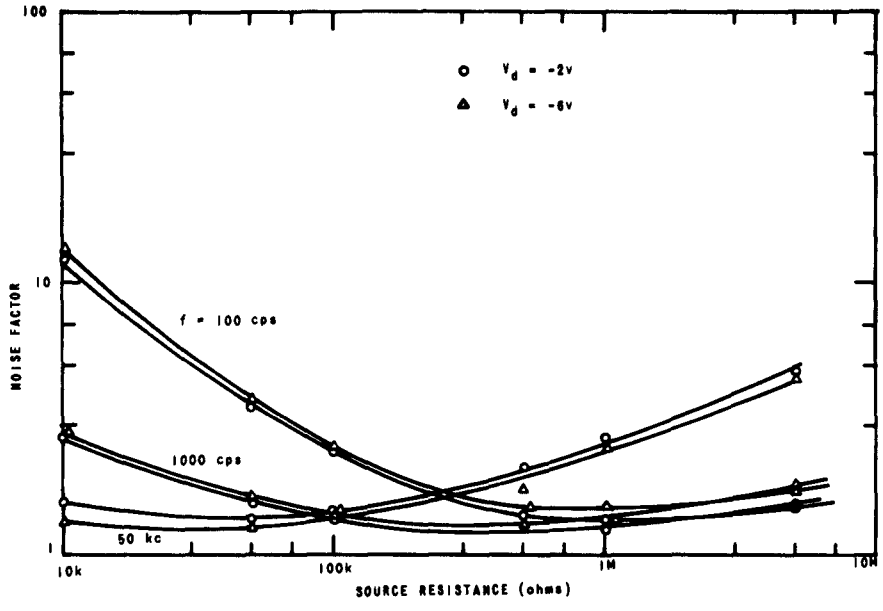


FIG. 36. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE TIX691 WITH FREQUENCY AND DRAIN BIAS AS PARAMETERS ($V_g$ = 0 v).

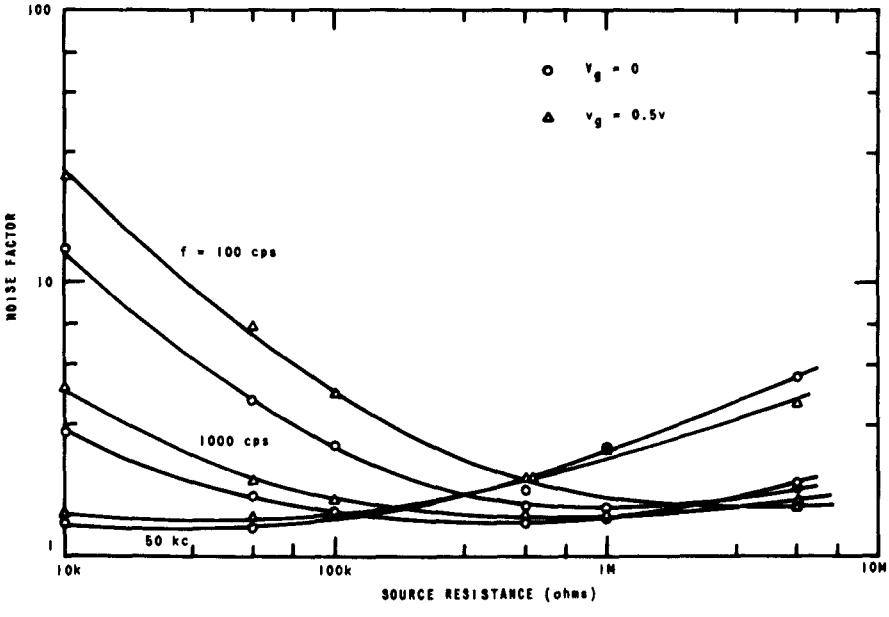


FIG. 37. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE TIX691 WITH FREQUENCY AND GATE BIAS AS PARAMETERS ($V_d$ = -6 v).

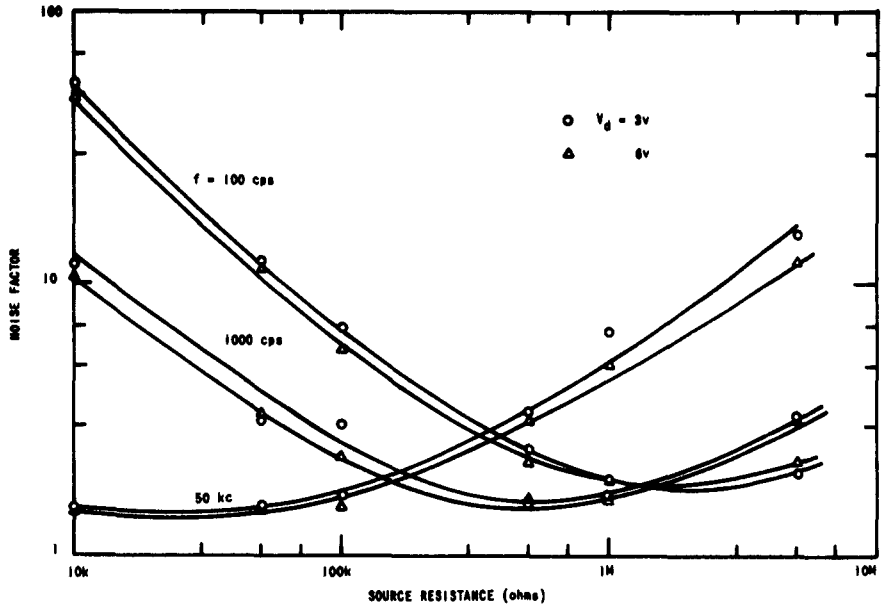


FIG. 38. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE C615 WITH FREQUENCY AND DRAIN BIAS AS PARAMETERS ($V_g$ = 0 v).

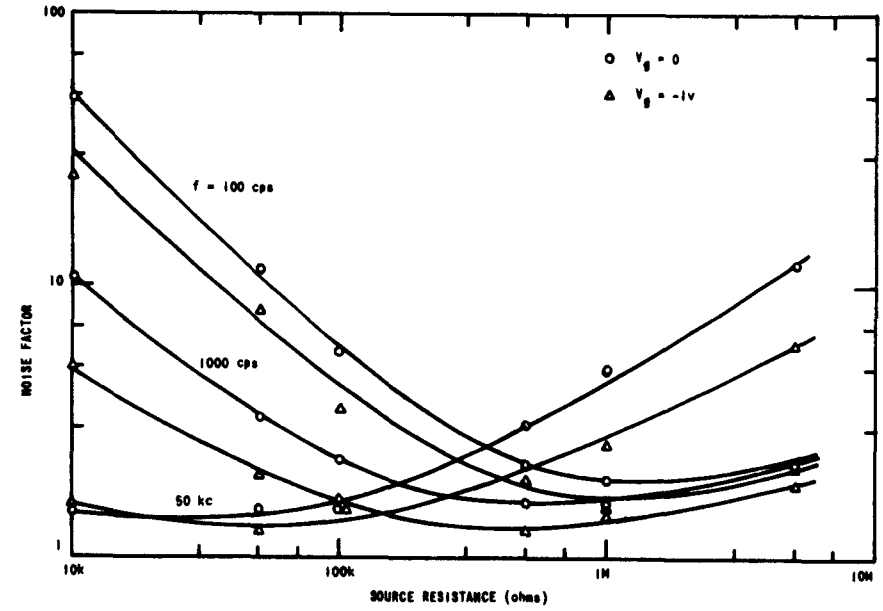


FIG. 39. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE C615 WITH FREQUENCY AND GATE BIAS AS PARAMETERS ($V_d$ = 6 v).

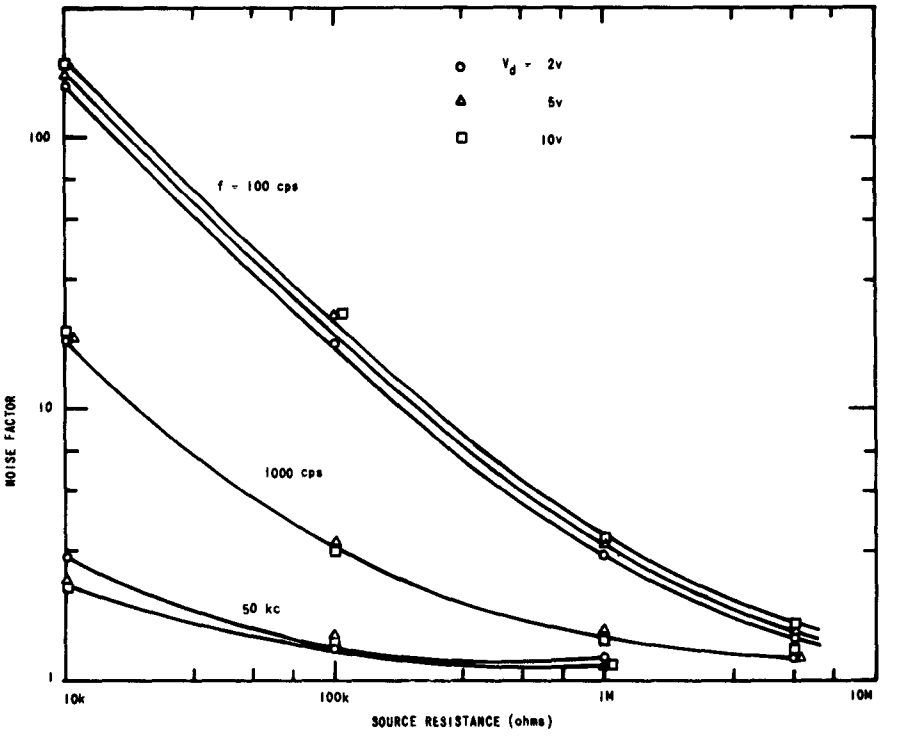


FIG. 40. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE FSP400 WITH FREQUENCY AND DRAIN BIAS AS PARAMETERS ($V_g$ = 0 v).

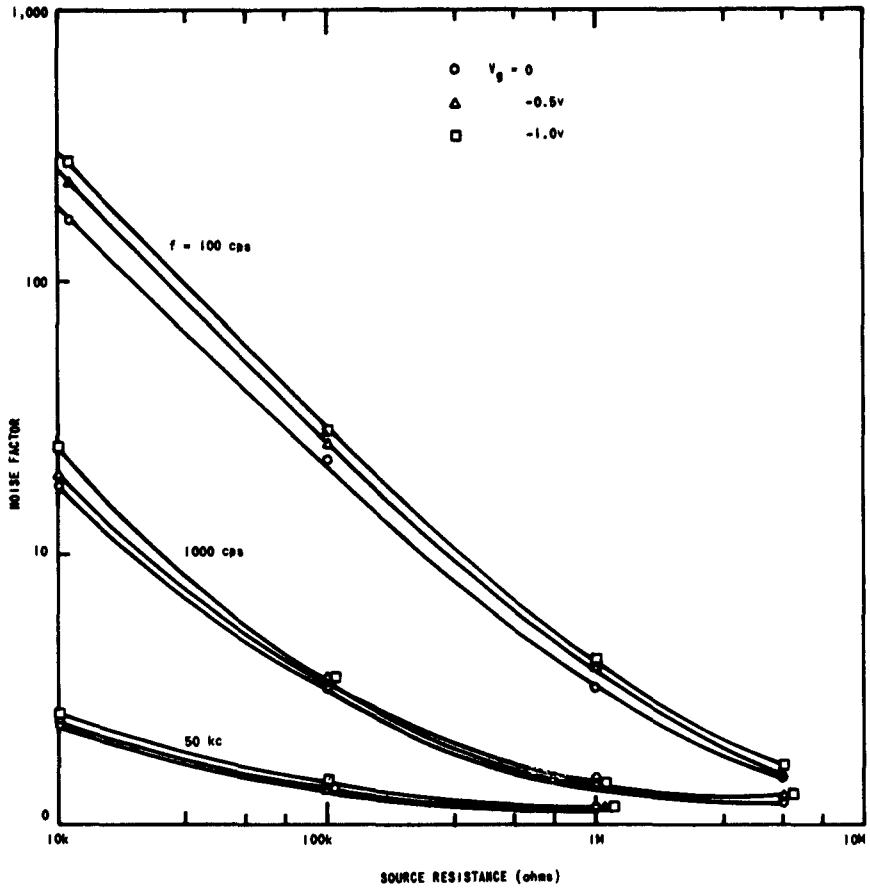


FIG. 41. NOISE FACTOR VS SOURCE RESISTANCE FOR DEVICE FSP400 WITH FREQUENCY AND GATE BIAS AS PARAMETERS ($V_d$ = 5 v).

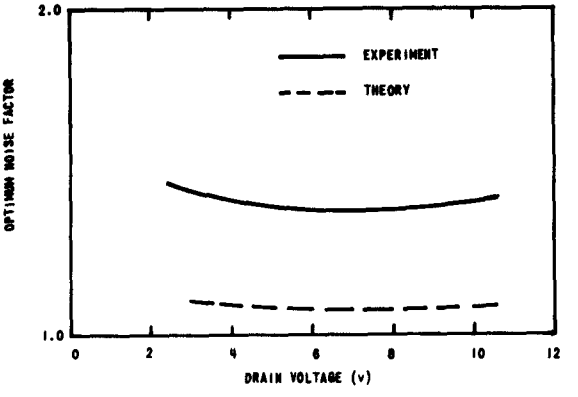


FIG. 42. OPTIMUM NOISE FACTOR VS DRAIN VOLTAGE FOR DEVICE C615 ($V_g$ = 0 v, f = 50 kc).

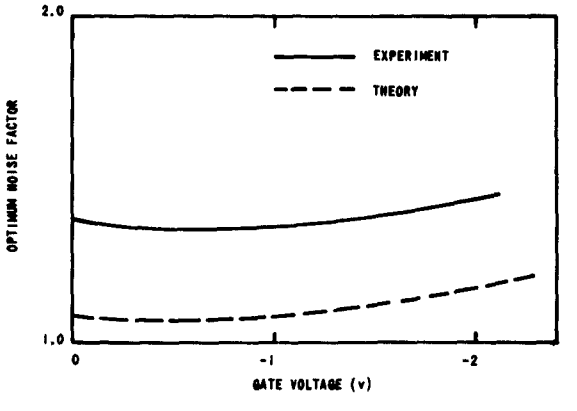


FIG. 43. OPTIMUM NOISE FACTOR VS GATE VOLTAGE FOR DEVICE C615 ($V_d$ = 6 v, f = 50 kc).

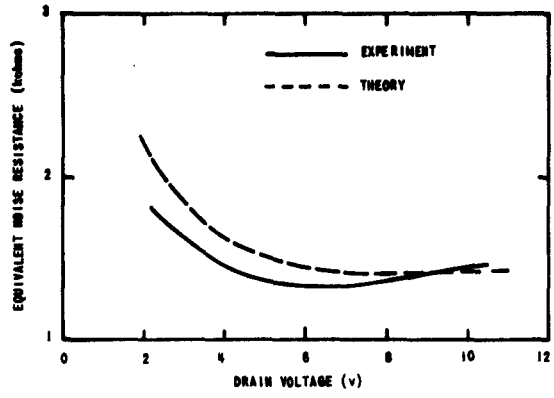


FIG. 44. EQUIVALENT NOISE RESISTANCE $R_n$ VS DRAIN VOLTAGE FOR DEVICE C615 ($V_g$ = 0 v, f = 50 kc).

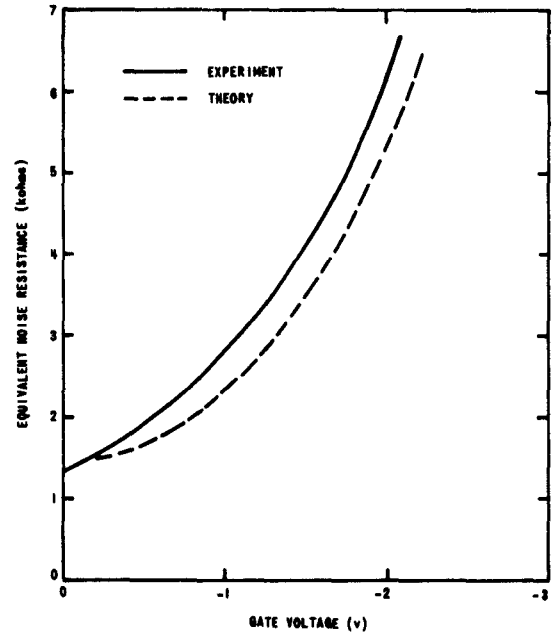


FIG. 45. EQUIVALENT NOISE RESISTANCE $R_n$ VS GATE VOLTAGE FOR DEVICE C615 ($V_d$ = 6 v, f = 50 kc).

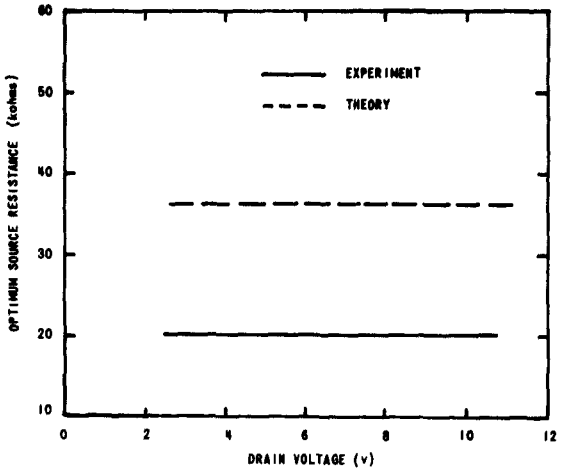


FIG. 46. OPTIMUM SOURCE RESISTANCE VS DRAIN VOLTAGE FOR DEVICE C615 ($V_g$ = 0 v, f = 50 kc).

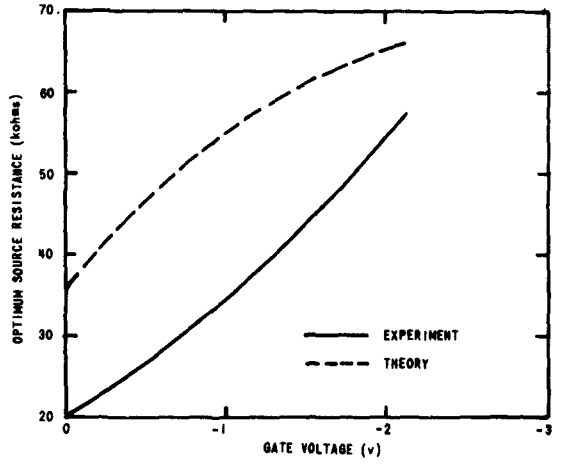


FIG. 47. OPTIMUM SOURCE RESISTANCE VS GATE VOLTAGE FOR DEVICE C615 ($V_d$ = 6 v, f = 50 kc).

## I. APPROXIMATE NOISE FACTOR IN 1/f NOISE REGION

If the source conductance is made much greater than the input admittance of the FET, then the noise factor can be approximated by

$$F = 1 + R_n G_s \tag{4.50}$$

In the 1/f noise region the output noise current decreases almost linearly with frequency to a frequency $f_1$ where the spectrum becomes essentially constant (cf. Fig. 31). This 1-f spectrum can be fitted by an empirical formula:

$$\overline{I_{n2}^2} = 4kT_o \lambda G_m \left(1 + \frac{f_1}{f}\right) \Delta f \tag{4.51}$$

Using (A.14) from the appendix an approximate form for the 1-f noise factor is

$$f = 1 + \frac{\lambda}{G_m} G_s \left(1 + \frac{f_1}{f}\right) \tag{4.52}$$

For the various devices $f_1$ is:

| | |
|---|---|
| C615: | 50 kc |
| TIX691: | 100 kc |
| FSP400: | 60 kc |

In addition the optimum drain bias for the minimum noise factor is less than the pinch-off voltage [cf. Figs. 16, 40] for devices with high 1-f noise. This observation seems to confirm Lauritzen's postulation of a high-field phenomenon as a cause of FET noise at low frequencies [Ref. 6].

## J. SUMMARY OF RESULTS

A noise model has been derived by assigning thermal-noise generators to the resistances of the transmission-line model and shot-noise generators to the gate junction. This resulted in a noise model characterized

by an equivalent input noise resistance inversely proportional to the transconductance of the device. For a resistive source the optimum source conductance was found to be approximately equal to the input admittance (output short-circuited).

# V. CONCLUSION

## A. APPLICATION OF THE MODELS

The principal results of this analysis have been a circuit model and a noise model of the field-effect transistor. Measurements have indicated that the circuit model is a useful representation for frequencies up to the cutoff frequency. Where 1/f noise is not present, noise measurements confirm the essential features of the noise model.

The similarity of the circuit and noise model of the field-effect transistor to those models of the vacuum-tube triode has been pointed out. The FET can therefore be used in any application where a triode is useful. Moreover, the FET has the advantage of a smaller equivalent noise resistance (neglecting 1/f noise contributions). However, the field-effect transistor has one of the same disadvantages of the triode, viz., a large feedback capacitance; this becomes important when the device is used as a high-frequency amplifier. The problem can be overcome by using a cascode connection, i.e., a grounded source stage followed by a grounded gate stage. In this case the FET yields a lower noise factor in comparison to the triode because of the smaller noise resistance and input conductance of the FET.

The most appropriate model for comparing the junction transistor (in the common-emitter connection) to the field-effect transistor is the pi-model. The major differences between the pi-models of the two devices are the input circuit elements. At low frequencies the junction-transistor input circuit is dominated by the input resistance (typically in the kilohm range), while the field-effect transistor input circuit is predominantly a capacitive reactance (typically in the megohm range). For this reason the junction transistor is most often used at low-impedance levels, while the field-effect transistor should find wide application at high impedance levels.

The high input impedance of the FET also engenders a lower noise factor for large values of source resistance. For a source resistance of 1 megohm a low-noise field-effect transistor can have a noise figure as low as 0.4 db [Ref. 6] while the junction transistor is rarely used

at such large source resistances. Moreover, the field-effect transistor can have a lower optimum noise factor than the junction transistor. In Chapter IV we found that

$$F_o = 1 + 2R_n G_o$$

For the FET we can assume $R_n$ = 1000 ohms, $G_o$ = 1 μmho; the junction transistor has an equivalent noise resistance about equal to the base resistance (usually about 50 ohms) and an optimum source resistance of 1 mmho. Substituting these values into the above equation we obtain

Junction transistor: $F_o = 0.4$ db

Field-effect transistor: $F_o = 0.02$ db

Thus, even considering the impedance levels, we find that the FET has a lower optimum noise factor.

## B. SUGGESTIONS FOR FURTHER STUDY

The approach used in this work was to approximate a transmission line with a two-section model. An exact solution to the FET wave equation can be obtained if the boundaries of the channel can be expressed effectively. Knowledge of the voltage and current at the ends of the line can be used to calculate the admittance parameters. Although the solutions will probably be transcendental functions, an approximation can be made at this point to yield a circuit model. The advantage of making the approximation at this point rather than at the outset is that the high-frequency parameters can be related directly to the dimensions and other physical constants of the device.

Further study should be directed toward an understanding of 1/f noise in these devices. Especially important would be knowledge of the relative sensitivity of the field-effect transistor to 1/f noise-producing mechanisms as compared to the junction transistor. Since both devices are used in low-level circuits, it would be advantageous to know which device had the lower 1/f noise.

## APPENDIX: A GENERAL REPRESENTATION OF NOISE IN LINEAR TWOPORTS [Ref. 14]

In many cases it is convenient to employ a noise representation where the device noise is represented by two generators at the input of the device. This representation is shown in Fig. 48.

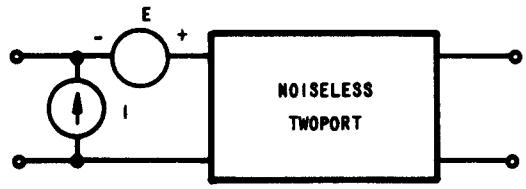


FIG. 48. TWO-GENERATOR NOISE MODEL.

For this representation the noise factor is

$$F = 1 + \frac{\overline{|I + Y_s E|^2}}{4kT_o G_s \Delta f} \tag{A.1}$$

Expanding, we obtain

$$F = 1 + \frac{\overline{I^2}}{4kT_o G_s \Delta f} + \frac{\overline{E^2}|Y_s|^2}{4kT_o G_s \Delta f} + \frac{\overline{E^* Y_s^* I} + \overline{E Y_s I^*}}{4kT_o G_s \Delta f}$$

Now define an uncorrelated noise current, $I_u$, such that

$$\overline{E I_u^*} = 0$$

$$(I - I_u) I_u^* = 0$$

Write

$$I - I_u \triangleq Y_\gamma E$$

$$Y_\gamma \triangleq G_\gamma + jB_\gamma$$

$Y_\gamma$ is called the correlation admittance. Then

$$\overline{EI^*} = Y_\gamma^* \overline{E^2} \tag{A.2}$$

An equivalent noise conductance $G_u$ and an equivalent noise resistance $R_n$ can be defined:

$$\overline{I_u^2} \triangleq 4kT_o G_u \Delta f \tag{A.3}$$

$$\overline{E^2} \triangleq 4kT_o R_n \Delta f \tag{A.4}$$

The fluctuations in the total noise current are

$$\overline{I^2} = 4kT_o \left[ |Y_\gamma|^2 R_n + G_u \right] \Delta f \tag{A.5}$$

In terms of these new variables the noise factor is

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s} \left[ (G_s + G_\gamma)^2 + (B_s + B_\gamma)^2 \right] \tag{A.6}$$

The minimum noise factor $F_o$ is obtained when the source conductance is

$$G_o = \left[ \frac{G_u + R_n G_\gamma^2}{R_n} \right]^{1/2} \tag{A.7}$$

and the source susceptance is

$$B_o = -B_\gamma \tag{A.8}$$

The value of this minimum noise factor is

$$F_o = 1 + 2R_n(G_\gamma + G_o) \tag{A.9}$$

A third form of the noise factor, in terms of $G_o$, $B_o$, $F_o$ and $R_n$, is

$$F = F_o + \frac{R_n}{G_s} \left[(G_s - G_o)^2 + (B_s - B_o)^2\right] \tag{A.10}$$

This result is important in that it holds for any linear twoport.

By measuring $F_o$, $G_o$, $B_o$, and $R_n$ for various bias conditions and frequencies, one can determine the noise generators E and I (and their correlation).

However, the noise model of the FET is based on noise generators at the input and output of the device (cf. Fig. 24). In this case the noise factor is

$$F = 1 + \frac{\overline{\left|I_{n1} - \frac{Y_{11}}{Y_{21}} I_{n2} - Y_s \frac{I_{n2}}{Y_{21}}\right|^2}}{4kT_o G_s \Delta f} \tag{A.11}$$

A comparison of the two representations yields

$$I = I_{n1} - \frac{Y_{11}}{Y_{21}} I_{n2} \tag{A.12}$$

$$E = - \frac{I_{n2}}{Y_{21}} \tag{A.13}$$

Hence

$$R_n = \frac{\overline{I_{n2}^2}}{4kT_o |Y_{21}|^2 \Delta f} \tag{A.14}$$

From (A.12) we infer

$$\overline{I^2} = \overline{I_{n1}^2} + \left|\frac{Y_{11}}{Y_{21}}\right|^2 \overline{I_{n2}^2} - \overline{I_{n1}^* \frac{Y_{11}}{Y_{21}} I_{n2}} - \overline{I_{n1} \frac{Y_{11}^*}{Y_{21}^*} I_{n2}} \tag{A.15}$$

Using (A.12) and (A.13), we obtain:

$$\overline{EI^*} = \frac{\overline{I_{n2}^2}}{|Y_{21}|^2} Y_{11}^* = Y_\gamma^* \overline{E^2} \tag{A.16}$$

Comparison shows:

$$Y_\gamma = Y_{11} \tag{A.17}$$

The uncorrelated noise current is obtained by subtracting $4kT_o|Y_\gamma|^2 R_n \Delta f$ from (A.15):

$$4kT_o G_u \Delta f = \overline{I_{n1}^2} - \overline{I_{n1}^* I_{n2}} \frac{Y_{11}}{Y_{21}} - \frac{Y_{11}^*}{Y_{21}^*} \overline{I_{n1} I_{n2}^*} \tag{A.18}$$

Thus $F_o$, $G_o$, $B_o$, and $R_n$ are found from $I_{n1}$, $I_{n2}$, and their correlation.

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